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SERIAL DRUM
24

INSTRUCTION MANUAL

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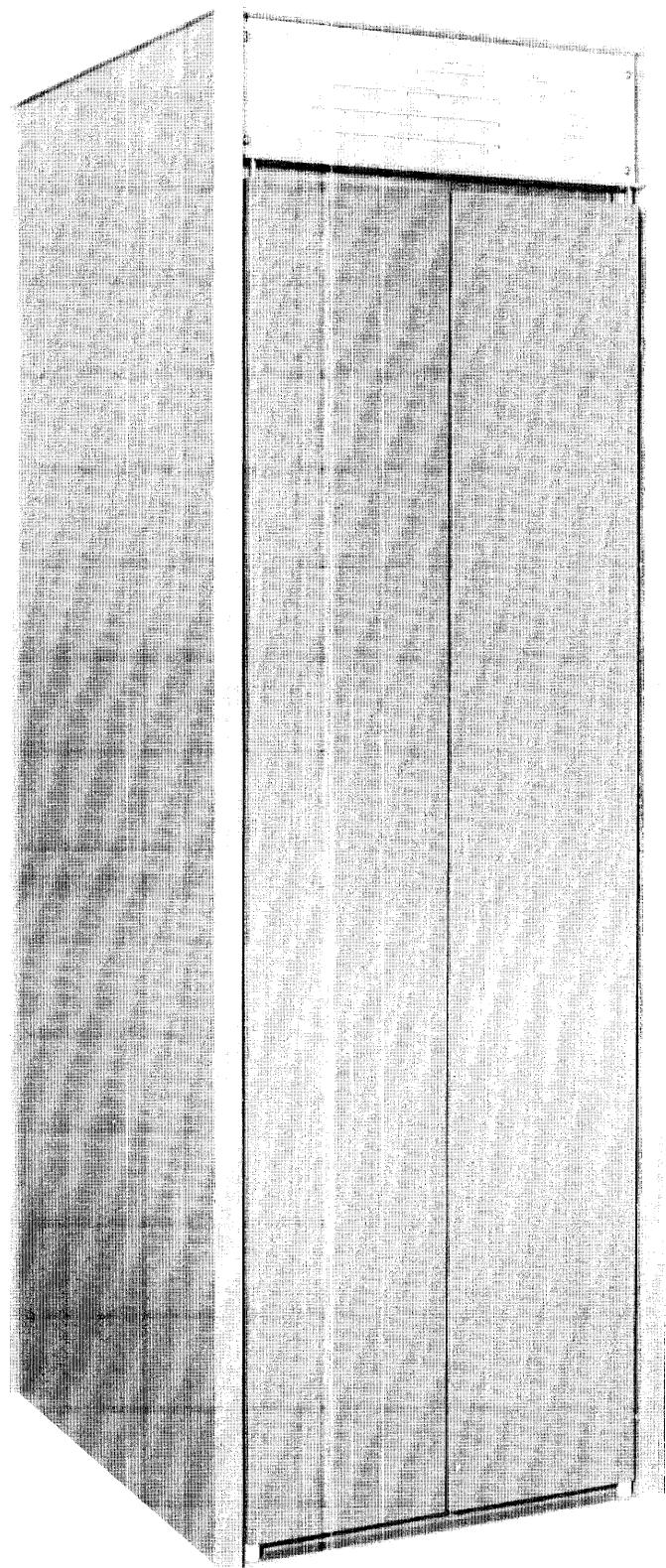
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Serial Drum Type 24

CHAPTER 1

INTRODUCTION

The Digital Equipment Corporation (DEC) Type 24 Serial Drum System serves as an auxiliary data storage device for programmed data processor PDP-1, PDP-4, and PDP-7. Information in the computer can be stored (written) in the serial drum and retrieved (read) in blocks of 256 computer words. After programmed initialization, 256-word blocks (sectors) of data are transferred automatically between the computer and the serial drum; transfer of each word is interleaved with the running computer program. Serial drums can store either 128, 256, or 512 data blocks, providing a memory capability of up to 131,032 computer words. Each word is transferred between the computer and the serial drum in parallel (18 bits at a time) and is written or read on the drum surface in series.

Since applications of the serial drum are more common in a PDP-4 computing system, this manual and the engineering drawings assume the machine is connected to a PDP-4. When the serial drum is connected to another computer, all references in this manual to signal origins and destinations and to data interrupt functions in the PDP-4 can be interpreted to refer to circuits performing similar functions.

FUNCTIONAL DESCRIPTION

The basic functions of the Type 24 Serial Drum are data storage and retrieval, core memory address control, track selection, data request and transfer control, error checking, and power supply distribution.

Under program control, the IOT (input-output transfer) instructions set up the drum control to transfer data. When the instructions specify the write cycle, a memory start address is set into a register in the serial drum. The memory address is incremented automatically after each word transfer to the serial drum from the computer. The track and sector address is also set into a register in the serial drum. The setup instruction initiates a data break cycle to transfer an 18-bit word to the serial drum from the addressed core memory location. A parity bit is generated for each 18-bit word so that a 19-bit word is written on the drum surface. After the 19-bit word is written, the data break cycle is entered to obtain the next word. Following the writing of the 256 words of the addressed sector, a flag is set to signify the completion of the sector transfer. The track and sector address register is incremented by one to simplify programming of continuous sector transfers.

When the program specifies a read cycle, a similar routine sets up the serial drum. The memory start address is set into the serial drum memory address register and the track and sector address is set into the serial drum track and sector address register. After a word is read from the addressed drum location, the

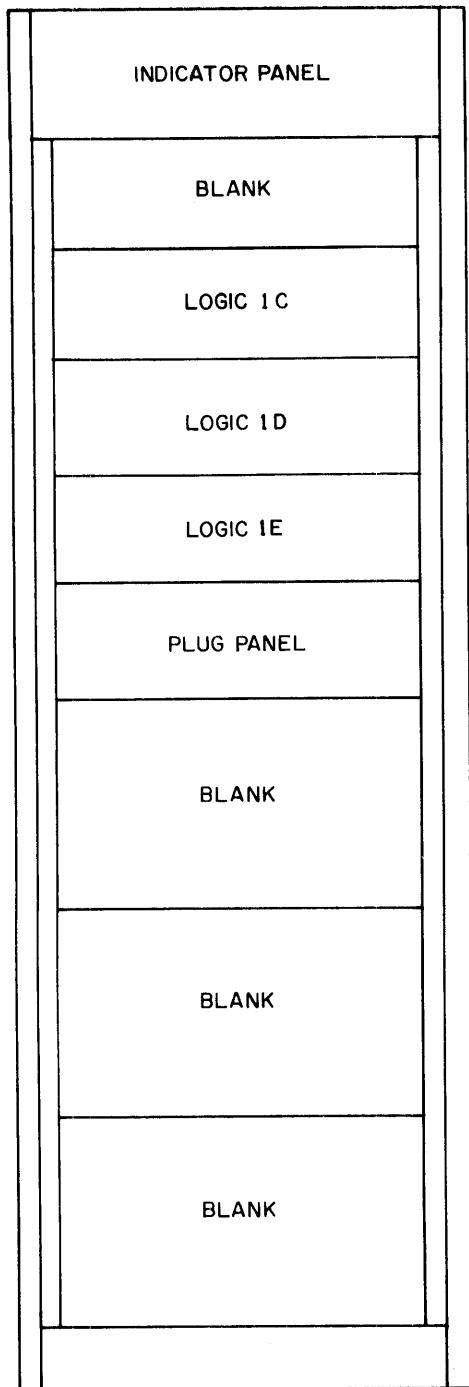
data break cycle is entered to transfer the word to core memory in the computer. When all 256 words of the addressed sector have been transferred, a flag is set to indicate the completion of the sector transfer.

Error circuits in the serial drum check for parity error during the read cycle and check data transmission timing errors during both read and write cycles. If bits are picked up or dropped out, if data received from the computer is late during a write cycle, or if data is late being stored in the core memory during a read cycle, an error signal is sent to the computer (when sensed by the program).

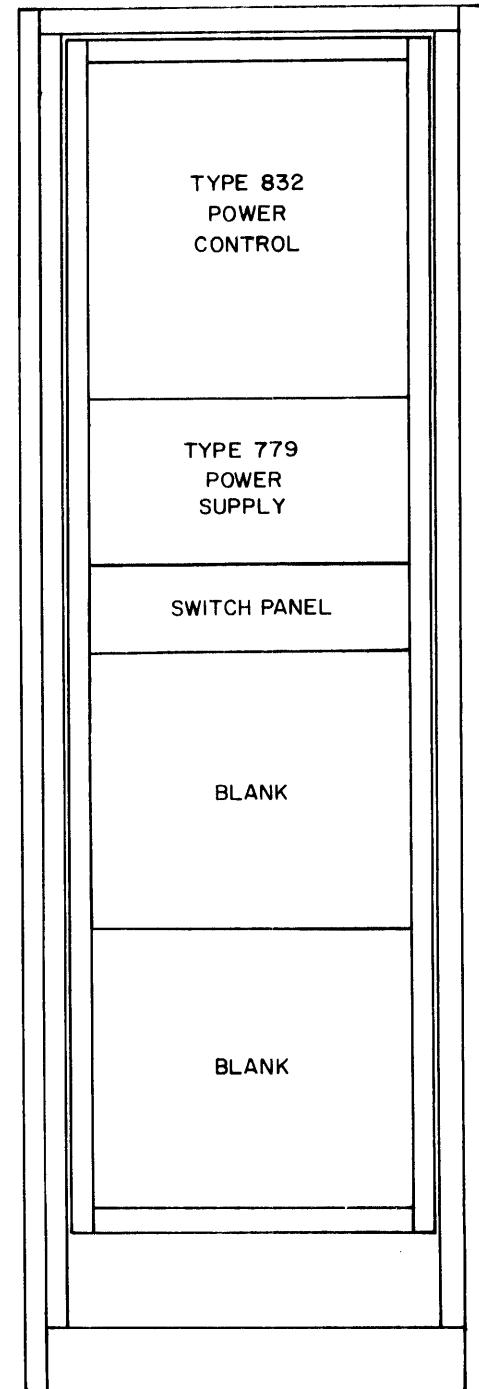
PHYSICAL DESCRIPTION

The Type 24 Serial Drum System is contained in a DEC computer cabinet 21-5/8 inches wide, 25-3/4 inches deep, and 67-7/16 inches high. All indicators are located on a panel at the front of the machine. Maintenance controls are located on the plenum door inside the double rear doors. Power and signal cables enter the cabinet through a port in the bottom. The power cable is permanently wired to the equipment, and the two signal cables mate with connectors which are mounted on the front of the cabinet, facing the center of the machine. Four casters allow mobility of the machine (which weighs 550 pounds). The cabinet is constructed of a welded steel frame covered with sheet steel. Double front and rear doors are held closed by magnetic latches. A full-width plenum door provides mounting for the power control, power supply, and switch panel inside the double rear doors. The plenum door is latched by a spring-loaded pin at the top. The indicator panel, racks of logic, and cable connector panel are attached to the front of the cabinet. Module racks are mounted on the front of the cabinet with the wiring side forward, so that modules are accessible for insertion or extraction by opening the plenum door at the rear. A fan mounted at the bottom of the cabinet draws cooling air through a dust filter and passes it over the electronic components. The memory drum housing is mounted on braces above the fan assembly.

A coordinate system is used to locate racks, modules, cable connectors, and terminals. Each 5-1/4 inch position on the front of the cabinet is assigned a capital letter, beginning with A at the top, as indicated on Figure 1-1. Modules are numbered from 1 through 25 from left to right in a rack, as viewed from the wiring side (front). Connectors are numbered from 1 through 6, from left to right as viewed from the front of the machine. Blank module and connector locations are not numbered. Terminals on a module connector are designated by capital letters from top to bottom. Therefore, D09E is in the fourth location from the top (D), the ninth module from the left (9), and the fifth terminal (E) from the top of the module. Components mounted on the plenum door are not identified by location. Engineering drawing E-10208 (Chapter 7) shows the system for locating terminal blocks and standoffs mounted on the logic racks.



FRONT VIEW



BACK VIEW

Figure 1-1 Component Locations

Specifications

Dimensions

23-1/2 inches wide
27-1/16 inches deep
69-1/8 inches high

Service Clearances	8-3/4 inches in front 14-7/8 inches in back
Weight	550 lbs
Power Required	115v, 60 cps, single phase, 8-amp starting current, 5-amp running current
Power Dissipation	450 watts
Power Control Point	Local or remote (computer)
Initial Starting Delay	5 min
Signal Cables	2, 50 wire, shielded
Temperature	32 to 105°F operating range
Drum Motor	115v, single phase, 2 pole, induction, capacitor start and run
Magnetic Head Interference	Maximum interchannel read cross talk at least 25 db below nominal signal level. Maximum noise in any channel at least 25 db below nominal signal level.
Write Current	100 ma
Pulse Repetition Rate	1.70 μ sec
Word Transfer Time	66.5 μ sec
Block Transfer Cycle (1 drum revolution)	17.3 msec

ABBREVIATIONS

The following abbreviations are used throughout this manual and on engineering drawings:

AC	Accumulator in computer
ACB	Buffered outputs of accumulator in computer
ACT	Active
AMP	Amplifier
AMPH	Amphenol connector
ANS	Answered

B	Break (computer state)
COMP	Complement
COND	Conditioned or enabled
DCL	Drum core location counter in serial drum
DCT	Drum control element in serial drum
DDC	Drum data channel in serial drum
DE	Data error
DF and DFB	Drum final buffer in serial drum
DIC	Data interrupt control in computer
ER SYNC	Error sync flip-flop
DS	Device selector in computer
DSB	Drum serial buffer in serial drum
DT and DTR	Drum track address register in serial drum
DTD	Drum track address decoder in serial drum
EXT	External
F	As a subscript means final or last bit of information; the bit after the least significant data word bit
FL	Field lockout
IOS	Input/output skip facility in computer
IOT	Input/output transfer
MA and MAR	Memory address register in computer
MB	Memory buffer register in computer
PA	Pulse amplifier
PAR	Parity
PC	Power control (Type 832)
PE	Parity error
PG	Pulse generator

PIC	Program interrupt control in computer
R	Read
RD/WR	Read/write flip-flop
RQ	Request flip-flop
R/WP	Read/write parity element in serial drum
S	As a subscript means the first or initial bit of information; the bit preceding the most significant data word bit
SA	Sector address
SEC CNT	Sector counter
STR ADD	Sector address
TRA	Transfer
WD	Write data flip-flop
WR ENA	Write enable
XA	Most significant octal digit of X address
XB	Least significant octal digit of X address
YA	Most significant octal digit of Y address
YB	Least significant octal digit of Y address

REFERENCE CONVENTIONS

The Digital Equipment Corporation engineering drawing conventions and instruction manual referencing should be understood at this point. A study of the material contained in Chapter 7 and the following paragraphs before proceeding with detailed descriptions will save considerable reference time and preserve thought continuity when reading the text that follows.

Any reference to an illustration by a chapter-oriented figure number indicates that the figure is to be found in text following the reference. Any reference to an engineering drawing number indicates that the drawing is to be found in a special drawing section or chapter. All engineering drawings are referenced first by the full drawing number.

Example: BS-D-24EFG-0-8

To locate a specific signal or function on a drawing, a system of coordinates is used. As shown on the drawings of Chapter 7, coordinates are designated by a number and letter. Thus, in any drawing reference, coordinate location appears immediately after the number separated by a colon.

Example: BS-D-24EFG-0-8:D1

To avoid needless repetition of the full drawing number, in-text references can use a short designation form that includes only the difference modifier(s) of the drawing designation plus the coordinates.

Example: -8:D1

One last text reference convention must be noted. Occasionally it is desirable to indicate the condition of a circuit within a logic description. As shown on the drawings of Chapter 7, circuit locations are identified. For reference in text, this designation is noted; for example, CB24. If the condition of the circuit is to be stated, the reference becomes either CB24(1) or CB24(0).

REFERENCE DOCUMENTS

Systems Modules Catalog, C-100

by Digital Equipment Corp.

FLIP CHIP Modules Catalog, C-105

by Digital Equipment Corp.

CHAPTER 2

PRINCIPLES OF OPERATION

RECORDING AND PLAYBACK TECHNIQUE

The recording and playback technique employed by the Type 24 Serial Drum is NRZ (non-return-to-zero) phase modulation. This technique records binary 1's and 0's by controlling the direction of flux change on the drum surface. For example, a flux change in one direction represents a 1, and a flux change in the opposite direction represents a 0.

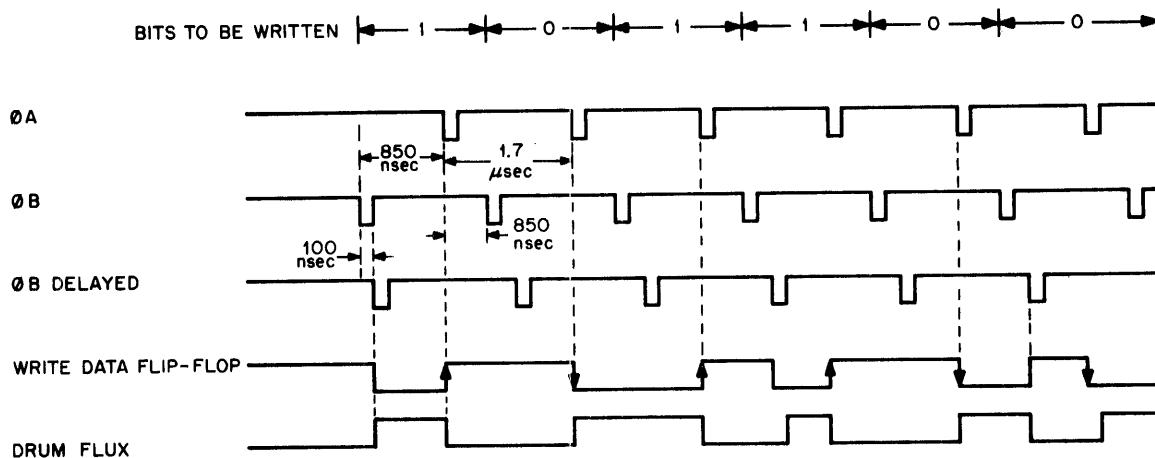


Figure 2-1 Simplified Timing of NRZ Writing

To clarify this point consider the timing diagram Figure 2-1 and the simplified logic diagram Figure 2-2. As shown on these drawings, a positive voltage swing (identified by the arrow) from the write flip-flop produces a flux change to write a 1, and a negative voltage swing produces a flux change in the opposite direction to write a 0. The read/write circuits are synchronized so that recording occurs on the phase A time pulse. The write flip-flop must be in a state (reset to write a 0 or set to write a 1) so that the phase A pulse can complement the flip-flop to write the specified bit. The phase B pulse shifts the bit to be written into the last bit of the data register, the DSBO flip-flop. The delayed phase B pulse senses the DSBO bit to put the write flip-flop into the proper state so that the next phase A pulse complements the write flip-flop to write the bit specified by DSBO.

Obviously, when the state of the write flip-flop is switched by the delayed phase B pulse, it causes a flux change on the drum surface. This flux change, however, is not sensed (two flux reversals per bit) because during playback (reading) the drum is sensed for a flux change only at phase A time. Detailed information on the principle of NRZ recording using phase modulation is shown in Figure 2-3.

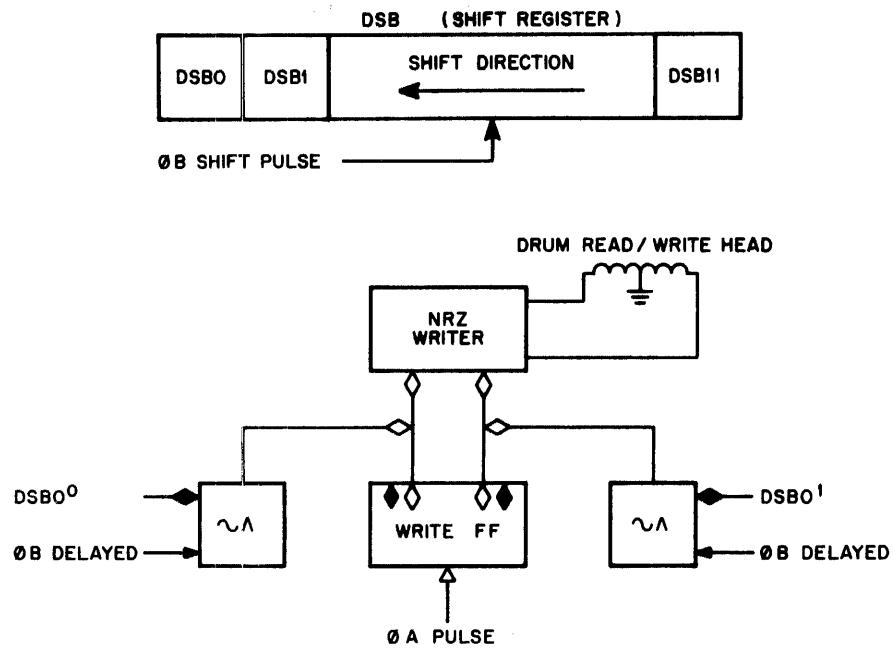


Figure 2-2 Simplified Logic of Writing Circuits

DRUM FORMAT

Data from the computer is written on drum tracks that circumscribe the drum cylinder as shown in Figure 2-4. The 24 Serial Drum Systems are available with 8, 16, 32, 64, 128, 192, or 256 tracks. Each data track contains 2 sectors, and each sector contains 256 19-bit words. The 19-bit word consists of 18 data bits plus a parity bit (used only in the drum system).

The words within a sector are not stored consecutively on the track; rather, every other word is peculiar to the same sector as shown in Figure 2-4. Each word is transferred to the drum serial buffer in approximately 34 μ sec; a sector transfer is completed in approximately 17.3 msec.

The drum also contains a clock pulse track. The clock pulse track supplies clock pulses to the drum control logic at 1.7- μ sec intervals to synchronize writing and reading of the drum. A 300- μ sec gap, where no clock pulses exist, separates the beginning and the end of each track.

Figure 2-5 shows a closer view of a typical 19-bit word. The word shown is the first word of the track, word 1 of sector 0. The first clock pulse (index pulse) following the 300- μ sec gap does not write a bit; it alerts the drum control circuits of the beginning of timing pulses. The next 18 drum clock pulses write the 18 data bits of the word. After 18 bits are written, an odd parity bit is written; i.e., if the 18 bits contain an even number of 1's, a parity bit of 1 is written to indicate odd parity. To separate words written on the drum, every 20th drum clock pulse does not write a bit, thereby providing a 3.5- μ sec-gap

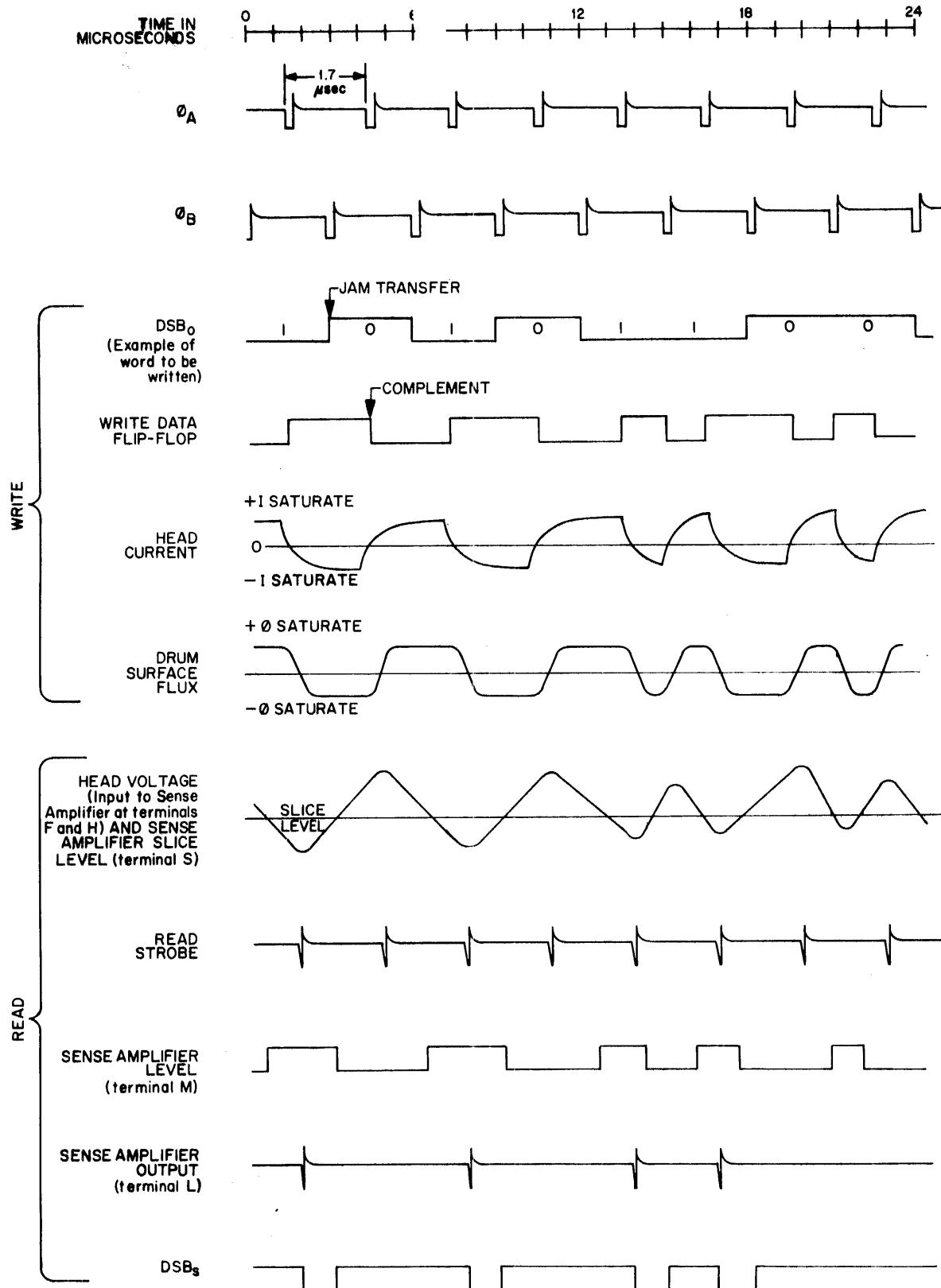


Figure 2-3 Typical Recording and Playback Timing

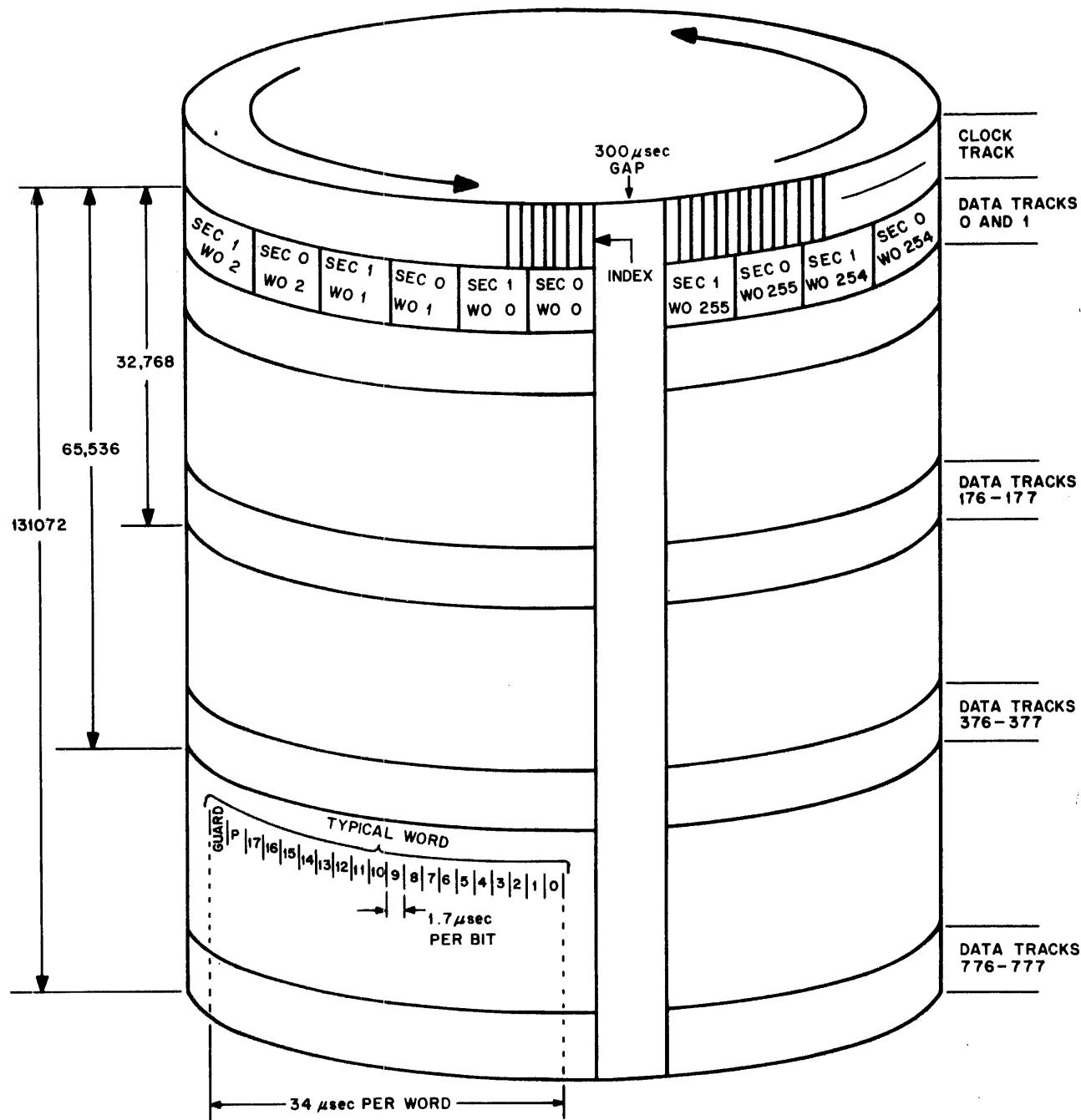


Figure 2-4 Drum Surface Format

between words. There are 20 drum clock pulses per word throughout the entire drum track. This remains true even though the first clock pulse does not record a bit. The last word written does not contain a gap and consequently no clock pulse is needed; therefore, it requires only 19 clock pulses. This makes up for the index pulse so that there are 20 clock pulses per word throughout the drum track.

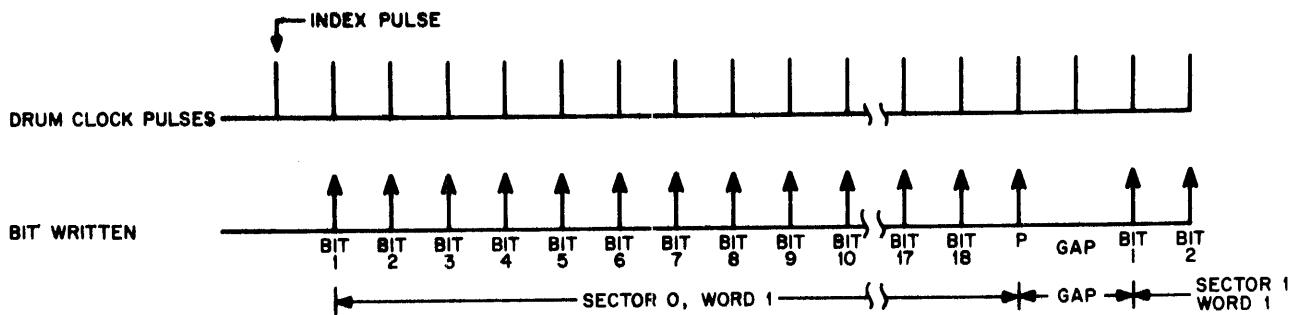


Figure 2-5 Sector Word Format

BLOCK DIAGRAM DISCUSSION

Major functional elements of the Serial Drum are shown in Figure 2-6. Complete information transfer flow and timing of operations in the serial drum are indicated in engineering drawings FD-D-24EFG-0-2 and TD-D24EFG-0-31.

Drum Core Location Counter (DCL)

The DCL is shown on engineering drawing BS-D-24604 to be a 16-bit flip-flop register which contains the computer core memory address to or from which the next word is to be transferred. Before transfer of the initial word in a block, the address of the first word is set into the DCL from the computer accumulator. As each word is transferred, the DCL is automatically incremented by one.

Drum Track Address Register (DTR)

The DTR is a 9-bit flip-flop register which contains the address of the drum track selected for transfer of a data block. The least significant bit is the sector address. The drum track (which may be considered as the data block address in the drum) is set into the serial drum, during program initialization, from the accumulator of the computer. At the completion of a successful block transfer (if the $DE^0 \cdot PE^0$ flag is a 0) the DTR is incremented by one to simplify programming of continuous transfers at successive drum tracks. Engineering drawing BS-D-24EFG-0-7 shows the DTR.

Drum Track Address Decoder (DTD)

Half of the drum track selection is performed by decoding of the DTR flip-flop outputs in the DTD. As shown on engineering drawing -7, the DTD consists of two groups of eight 2-input diode gates, one group for the X address and one for the Y address. The eight X address outputs function as a 2-digit octal address which is further decoded in the drum X select logic. The eight Y address outputs serve a similar function.

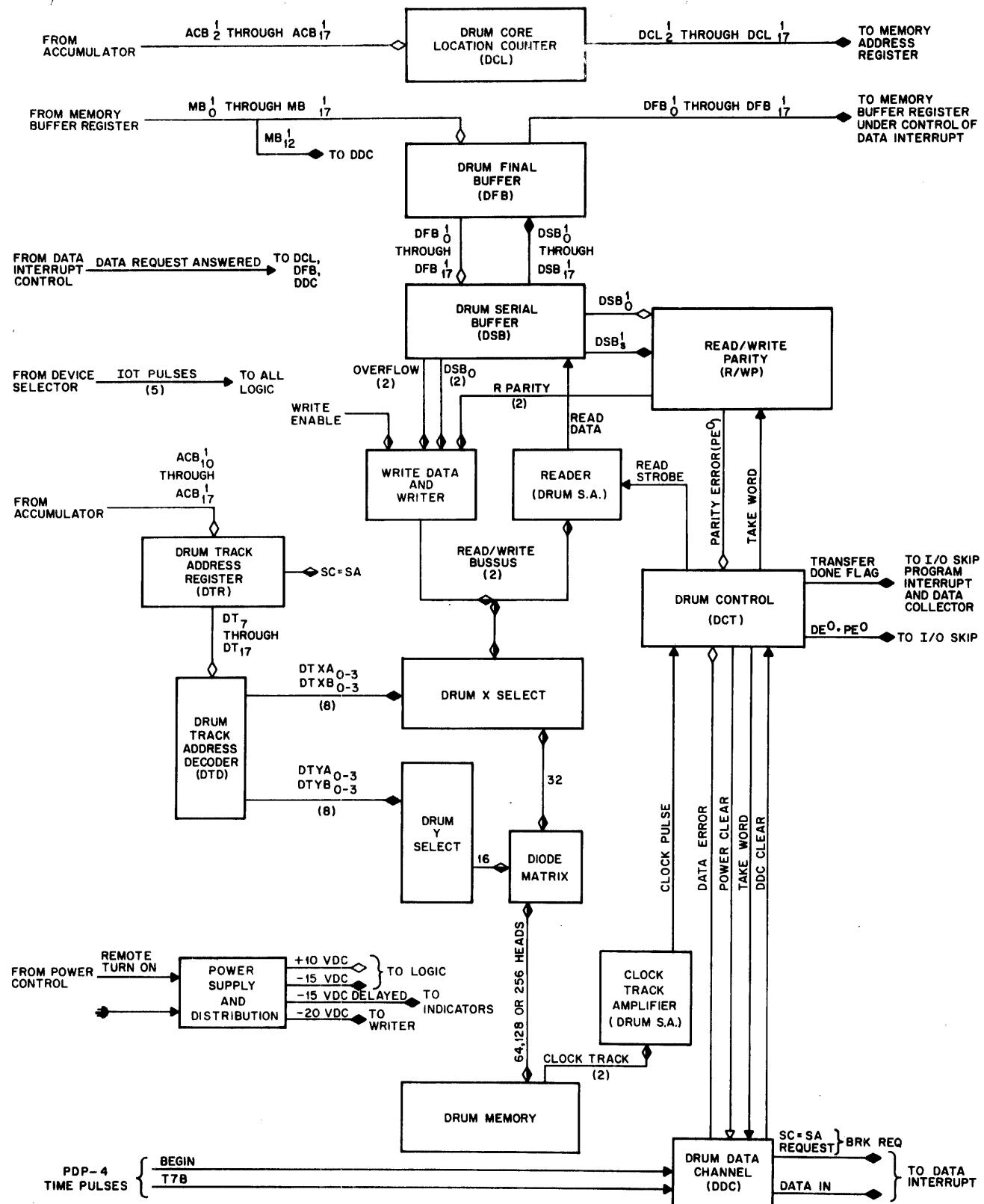


Figure 2-6 Type 24 Serial Drum Block Diagram

Drum Head Selection

Final selection of a drum head is performed in the drum X and Y select circuits shown on engineering drawing BS-E-24EFG-0-13 and in the diode matrix within the drum housing. Each of the 32 field lockout switches inhibits the writing on 8 tracks or 4096 words of drum memory.

Drum Sense Amplifiers

Two Type 1537 Drum Sense Amplifier modules convert information sensed by the magnetic heads of the drum into digital pulse data. Information recorded on a clock track is sensed by the clock head and supplied to the sense amplifier shown on drawing BS-D-24EFG-0-8 as the clock track amplifier. The output from this sense amplifier is applied to the drum control (DCT) to establish the basic clock rate of all drum operations. The sense amplifier shown on drawing BS-D-24EFG-0-10 as the READER samples the signals picked up by the selected data head and produces a pulse to set a 1 into the drum serial buffer (DSB) when the read strobe signal occurs during the maximum negative excursion of the head signal.

Drum Control (DCT)

The basic timing pulses for the machine are generated in the DCT from pulses received from the clock track amplifier. The DCT contains the sector counter and sector equality logic. The DCT also contains a 4-state device consisting of four negative diode gates. Each state of this device corresponds with and initiates one of the four machine control states: idle, transfer, active, or transfer done. This logic is shown on engineering drawing -8.

Drum Data Control (DDC)

Engineering drawing -11 shows the DDC. Circuits within the DDC control the transfer of each word between the computer and the drum serial buffer. The DDC establishes the read/write status of the machine, makes the data break request for a computer break cycle, indicates the detection of an error, and designates the direction of the ensuing data transfer.

Drum Final Buffer (DFB)

The DFB is an 18-bit register which serves as a buffer between the computer memory buffer register and the drum serial buffer. Words are transferred in parallel (18 bits at a time) under control of the computer data interrupt control. During drum writing, the DFB holds the next word. During drum reading, the DFB is empty and is prepared to accept information read from the DSB and place it into core memory under control of the data interrupt control. The logic circuits which compose the DFB are shown on engineering drawing D-24EFG-0-9.

Drum Serial Buffer (DSB)

As shown on the top and left side of engineering drawing -10, the DSB is an 18-bit shift register which is a serial-to-parallel converter during drum reading, and a parallel-to-serial converter during drum writing. Information is read from the drum into the DSB serially and transferred to the DFB in parallel. During drum writing, a word is read from the DFB into the DSB and written serially around the drum.

Read/Write Parity (R/WP)

As each bit of a word is written on the surface of the drum, the R parity flip-flop counts the number of binary 1's and produces a 19th bit to provide odd parity. When data is read from the drum, this flip-flop counts the 1's again and sets the parity error flip-flop if an even number is detected in any one word. The condition of the parity error flip-flop is indicated in the DCT as one of the two possible causes of an error condition. These circuits are shown on engineering drawing -10:C4,C5.

DRUM WRITE CYCLE

In general, the DRLCWR instruction (see Table 5-1, Chapter 5) initiates a drum write cycle in the drum control logic. The DRLCWR instruction normalizes certain control flip-flops in the drum control logic, sets the read/write flip-flop to the write state, sets the drum 4-state device to IDLE, sets the data in/out signal to out (which notifies the computer data break circuits that the data transfer direction is out of the computer), loads the DCL register from the accumulator, and sets the break request flip-flop to initiate a data break (see engineering drawing -8).

NOTE: The drum control logic incorporates a 4-state device to signify drum control status. The four states are IDLE, TRA, ACT, and FLAG. Only one state is entered at a time, and during a normal transfer the states advance in sequence. Entry into any state disables all others. The IDLE state indicates that the drum has not been activated by the program or it is waiting a 200- μ sec delay to set the TRA state. The TRA state indicates that the drum control is set up to transfer data, but it must wait until the beginning of the track. The ACT state is entered at the beginning of the track to transfer data. The FLAG state indicates the completion of a sector transfer.

The break request signal, generated by the break request flip-flop, initiates a computer data break cycle. During the data break cycle, the DFB is loaded from the memory location specified by the DCL register; following this transfer the DCL register is incremented so that it addresses the next sequential memory location for the next data break cycle. The drum control circuits now wait for the execution of the DRLBLK instruction.

The DRLBLK instruction loads the drum track and sector address from the accumulator into the DT and SA register. The DT address register selects the specified track for the ensuing write cycle, and the SA specifies the sector. The DRLBLK then initiates the 200- μ sec delay which permits the track selection circuits to set up.

After the 200- μ sec delay, the TRA (transfer) state is set. The circuits now wait for the index pulse to signify the beginning of the track. The index pulse (first clock pulse after the 300- μ sec gap on the drum) sets the 4-state device to ACT (active), and if the sector counter is equal to the sector address (SC=SA), writing begins immediately. If SC \neq SA, writing is inhibited until SC=SA. Even though SC may not be equal to SA, all operations of writing are performed except that the NRZ writer is disabled. For example, the ACT signal enables the drum clock pulses to generate the shift pulses and the write pulses (phase A pulses). The first word to be written is shifted in the DSB by the shift pulses.

After a data bit is shifted into the most significant bit of the DSB (DSB0), the phase A pulse complements the write data flip-flop. If the NRZ writer is enabled, the data bit in DSB0 is written on the drum; if the NRZ writer is disabled, writing is simulated only. The control pulses continue shifting the contents of the DSB and writing the DSB0 contents (or simulate writing) until the 18 data bits and the parity bit are written. After the 19 bits are written, the DSB is again loaded from the DFB and the circuits are set up to write another word. At this point, the SC is incremented and if SC=SA, the NRZ writer is enabled and the break request is sent to the computer to reload the DFB with the next word to be written. Writing continues in this manner until all 256 words of a sector are written. The end of track (beginning of the 300- μ sec gap) sets the drum 4-state device to FLAG to indicate the completion of a sector transfer.

Writing One Sector

The DRLCWR command (see Table 5-1, Chapter 5) executed by the computer starts the write cycle. The execution of this command generates IOT 6002 and IOT 6004 pulses which occur at event times 0 and 2, respectively. (Refer to the PDP-4 computer handbook for the explanation of the IOT instructions.) The IOT 6002 and IOT 6004 pulses are coupled to the drum control logic. The functions performed by these pulses are outlined in Table 2-1 (located at the end of this chapter). The location column in Table 2-1 shows the location of the circuit on the engineering drawings. For example, -9:D1 refers to engineering drawing D-24EFG-0-9, coordinates D1.

After the DRLCWR execution, the DCL register contains the memory address of the first word to be written on the drum. The DRLCWR has set the break request flip-flop; therefore, the computer executes a data break (Table 2-1) to load the DFB from the memory location specified by the DCL register. The contents of the DCL register are incremented so that it addresses the next sequential memory location.

The control circuits now wait for the computer to execute the DRLBLK instruction. The DRLBLK instruction generates IOT 6102 and IOT 6104 pulses. These pulses perform the operations outlined in Table 2-1. In brief, they load the DT and SA register from the accumulator, transfer the contents of the DFB into DSB, and trigger the 200- μ sec delay which sets the TRA state.

The DSB is loaded with the word to be written, and assuming that the 200- μ sec delay (-8:C2) is complete, the 4-state device is set to TRA. At this point the position of the drum is not known; therefore, the circuits must wait for the index pulse to signify the beginning of the drum track. Note that no phase A (ϕ A) or phase B (ϕ B) pulses are generated since ACT=0 (1D18U, -8:C3). Therefore, the DSB is not shifted and no writing occurs.

It should be noted that if sector 0 is addressed, the DRLBLK instruction that loads the DT and SA address also initiates a data break cycle to transfer the second word to be written into the DFB. This is because the sector counter is clear and SC=SA. The TAKE WORD signal (generated during DRLBLK) is enabled by SC=SA (-11:B2/3) to set the break request (RQ) flip-flop. Also, the DF \rightarrow DSB signal (generated by DSBINI COND1 μ sec, \rightarrow 10:C2) enables the WRITE ENABLE flip-flop (-10:D8) since SC=SA. Consequently, when sector 0 is addressed, at the beginning of the drum track the DSB contains the first word to be written, the DFB contains the second word to be written, and the WRITE ENABLE flip-flop is enabled.

The index pulse generates the START pulse (-8:C4) which sets the 4-state device to the ACT state. The drum clock pulses are shaped by PG 1410 (-8:C2) whose output triggers the DONE/START 3.4- μ sec integrating single-shot multivibrator. As long as there are clock pulses, the DONE/START multivibrator is held in the START state. However, in the absence of drum clock pulses, for example, during the 300- μ sec gap, the DONE state is enforced. Hence, the index pulse sets the single-shot multivibrator to the START state, which in turn sets the 4-state device to ACT (-8:B2). (Refer to timing diagram Figure 2-7.) The ACT signal (-10:D5) generates the ACT+ ϕ B pulse. This pulse enables the WRITE DATA circuits (-10:D6/7) to put the WRITE DATA flip-flop (-10:C5) into the proper state to write the designated DSB0 bit at phase A pulse time. The ACT signal that gates the phase A pulse (-8:C3/4) does not permit the index pulse to generate a phase A pulse.

The second drum clock pulse generates the phase A pulse, and it complements the WRITE DATA flip-flop to produce the proper phase change. The WRITE DATA flip-flop output is coupled to the NRZ writer (Type 4529 module, -10:C8) to write the designated bit. The NRZ writer output is coupled through an isolation network to the read/write busses and to the selected drum read/write head. The ensuing phase B pulse, delayed to permit rise time of DSB0, generates the ACT+ ϕ B pulse which again establishes the proper state of the WRITE DATA flip-flop. The next phase A pulse writes the second bit specified by the DSB0 flip-flop.

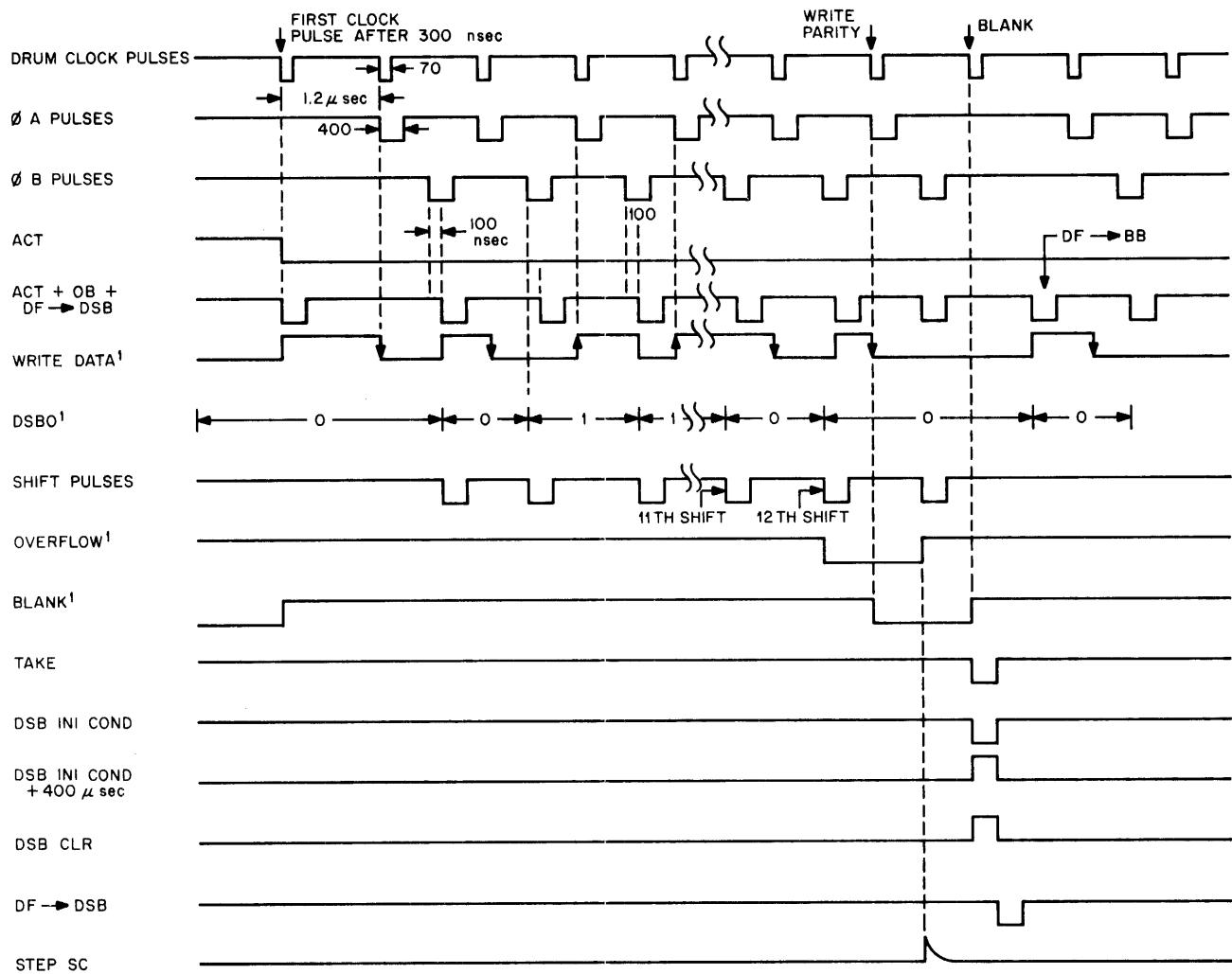


Figure 2-7 Write Cycle Timing

After 17 shifts of the DSB register, DSB2 through DSB17 contain all 0's because the DSBS flip-flop, which is continually reset by the shift pulses, shifts 0's into the DSB. Note that the DF \rightarrow DSB (DSB DF1 \rightarrow DSB) pulse initially sets DSBS; this insures a 1 bit in DSB2 through DSB17 during the 17 shifts, when a word is written. The 18th shift pulse sets the OVERFLOW flip-flop (-10:C4) since DSB2 through DSB17 are all 0's. The OVERFLOW signal enables the R PARITY flip-flop output (-10:D6/7) to write the parity bit. The shift pulses complement the R PARITY flip-flop for each 1 bit that is written. Since the R PARITY flip-flop is initially set, an odd number of 1's leaves the R PARITY flip-flop in the reset state. In this case, the R PARITY⁰ signal (1D10-M, -10:D6) enables the ACT+ØB pulse to reset the WRITE DATA flip-flop so that the ØA pulse writes a 0 parity bit to generate odd parity.

With the OVERFLOW flip-flop set, the next phase A (19th ØA) pulse sets the BLANK flip-flop (-8:D4). The BLANK flip-flop inhibits the phase A (20th ØA) and phase B (20th ØB) pulse for one drum clock period

(1D18V, -8:C4). Hence, a blank space (gap) separates the words written on the drum. The next phase B (19th \emptyset B) pulse resets the OVERFLOW flip-flop, and the next drum clock pulse resets the BLANK flip-flop. When the last word on the track is written, the BLANK flip-flop remains set since there are no more clock pulses to reset BLANK.

If the $SC \neq SA$, the action described above still occurs; however, the WRITE ENABLE flip-flop (-10:D8) is not enabled and no writing actually occurs on the drum.

As the OVERFLOW flip-flop is reset by the 19th phase B pulse, the trailing edge of the OVERFLOW signal (-8:B3) increments the sector count. As the BLANK flip-flop is reset, the $BLANK^0$ (BK^0) signal (-10:C1/2) generates the TAKE WORD signal which prepares the control circuits to write the next 19-bit word. (Refer to Table 2-1 for the sequence of events following the TAKE WORD signal.) Note that the DF \rightarrow DSB pulse (-10:D5) generates the ACT+ \emptyset B pulse that prepares the WRITE DATA flip-flop to write the first bit of the next word. If the $SC=SA$, the TAKE WORD signal (-11:B2) sets the RQ flip-flop to initiate a data break cycle to reload the DFB register.

Writing continues until all 256 words of the addressed sector are written. The drum clock pulse that writes the parity bit of the 256th word of sector 1 (whether the NRZ writer is enabled or not) is the last drum clock pulse before the 300- μ sec gap. The DONE/START one-shot multivibrator (-8:C4) reverts to the DONE state 3.4 μ sec after the last drum clock pulse. The DONE signal (-8:B3) sets the 4-state device to the FLAG state. The ACT signal (-7:D1) generates the DT+1 pulse which increments the SA register (-7:C8) so that the next sector (or track if $SA=1$) is addressed in case continuous sector transfers are specified by the program.

After the FLAG state is set, the actions that follow depend upon the computer program. If the computer is programmed to write only one sector, the program probably will check to see if a parity error or a data error occurred during the transfer. This is accomplished by DRSOK which skips the next instruction if the $DE^0 \cdot PE^0$ signal is 0; this permits the program to skip the next instruction and exit from the drum write subroutine if no parity or data errors exist. If an error exists, the next instruction executed will be a jump-to-error-check routine.

Writing Two Consecutive Sectors

When the computer is programmed to write more than one sector, instead of exiting from the write routine after one sector is written, the DRCONT* instruction causes writing to continue to the next sector. The DRCONT instruction (refer to Table 2-1) resets the PAR ERROR and DE flip-flops, generates TAKE WORD

*The DRCONT instruction can be given any time during the 300- μ sec gap which follows the previous written sector.

to prepare the control circuits to write the next word, and sets the 4-state device to TRA. With TRA set, the next index pulse sets the DONE/START multivibrator to START, which in turn sets the ACT state. The ACT signal enables the drum control circuits to write the next sector.

NOTE: Because the drum track selection circuits require a 200- μ sec stabilization time, a new track must be specified during the first 100 μ sec of the 300- μ sec gap.

READ CYCLE

The DRLCWR instruction (refer to Table 5-1, Chapter 5) loads the DCL register from the accumulator, normalizes control flip-flops in preparation for the read cycle, sets the 4-state device to IDLE, sets the DATA IN/OUT signal to DATA IN, and sets the READ/WRITE flip-flop to READ. The program executes the DRLBLK to load the DT and SA register from the accumulator, and after a 200 μ sec delay sets the TRA state. The next index pulse sets the ACT state, which enables the drum control circuits to read the drum. Data read from the addressed drum track is strobed into the least significant bit of the DSB register and the contents of the DSB are shifted. After 18 shifts the DSB contains the word read from the drum; then parity is checked. If a parity error occurs, the parity error flip-flop is set to indicate the error. If the SC=SA, the DSB contents are transferred to the DFB and the break request signal is sent to the computer.

The computer enters a data break cycle to transfer the DFB contents into the memory location specified by the DCL register. The DCL contents are then incremented. Transfer continues in this manner until all 256 words of the addressed sector are read. After the last word on the drum track is encountered, the FLAG state is set to signify the completion of the sector transfer.

Reading One Sector

The DRLCRD instruction (octal code 706606) generates the IOT 6002 and 6004 pulses. Table 2-2 shows the detailed signal flow of these IOT pulses. In brief, they set the IDLE state, clear the RD/WT (read/write) flip-flop, and load the core memory start address into the DCL from the computer accumulator. Note that the MB_{12} bit will be 0 to signify the read mode; consequently the IOT 6004 (-11:B2/3) does not set the RD/WT, RQ, and ER SYNC flip-flops. The RD/WT flip-flop remains clear to signify the READ state (-11:D2). The READ signal causes the DATA IN signal (-11:C2) to be -3v to signify a DATA IN direction to the data break circuits in the computer.

The DRLBLK instruction is then executed to load the DT and SA register with the drum track and sector address of the forthcoming read cycle. As shown in Table 2-2, the DRLBLK instruction prepares the control circuits to read the first word. Note that a 1 is inserted into DSB17 (by DSBINI COND+1 μ sec, -10:B8) after the DSB register is cleared. After 18 shifts (during which a word is read from drum), the 1 that was inserted into DSB17 is in DSF (-10:B1). Therefore, the DSF signal indicates that a word has been read from the drum.

After the 200- μ sec delay has elapsed and TRA is set, the control circuits wait for the index pulse. The index pulse sets the DONE/START one-shot multivibrator (-8:B4) to START, which in turn sets the 4-state device to ACT (-8:B2) (refer to Figure 2-8). The ACT signal (-8:C3/4) enables the drum clock pulses to produce phase A (\emptyset A), READ STROBE, and phase B (\emptyset B) pulses.

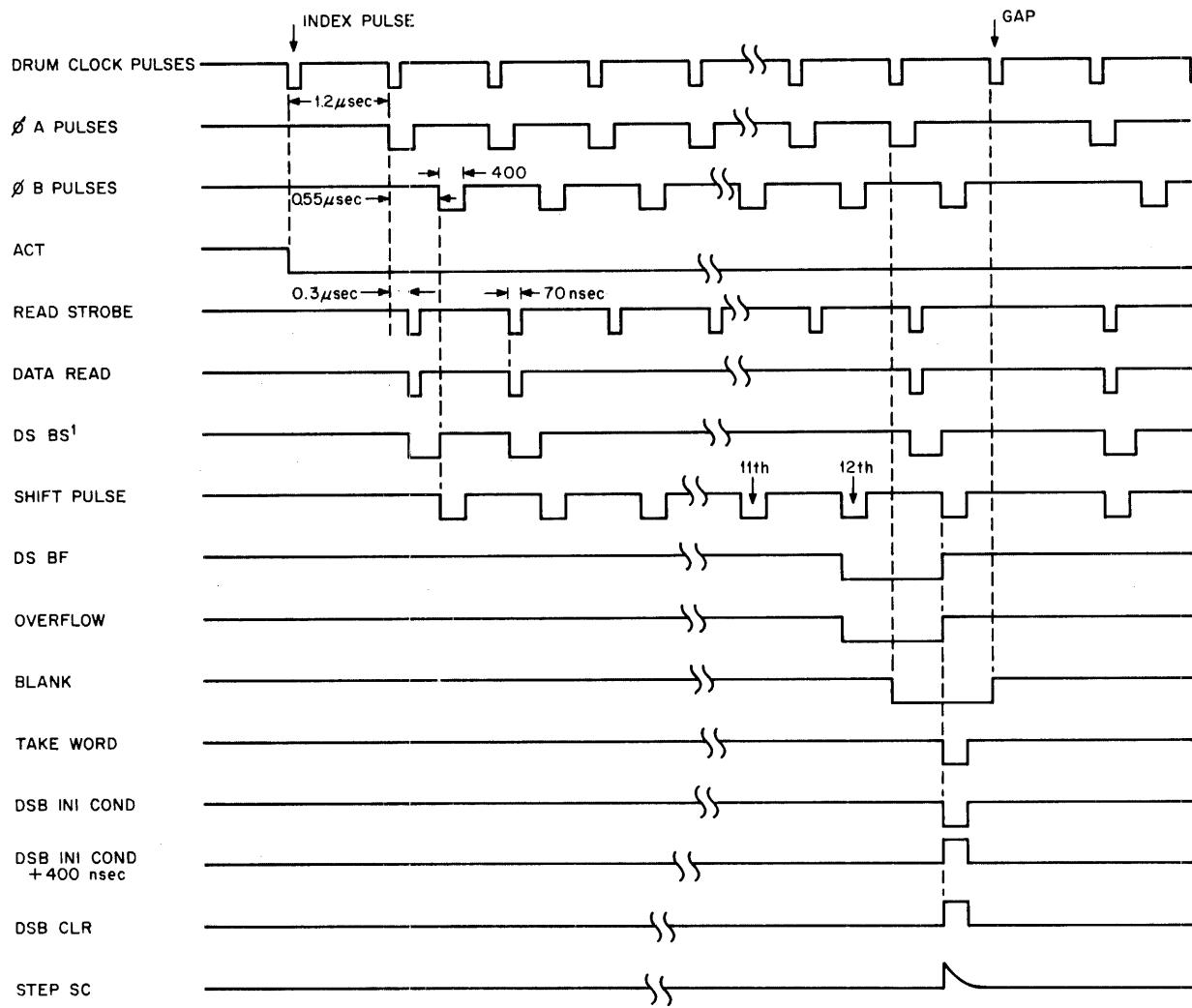


Figure 2-8 Read Cycle Timing

As the drum rotates, the flux changes induce signals into the read heads. The addressed drum read head output is applied to the Type 1537 Sense Amplifier. The READ STROBE, which occurs 0.3 μ sec after the phase A pulse, senses the sense amplifier (-10:C7) and produces a DATA READ pulse (E24L, -10:C7) when a 1 is read from the drum head; no pulse is produced when a 0 is read from the drum head. The DATA READ pulse sets the DSBS flip-flop (-10:B8), and the next shift pulse shifts the 1 from the DSBS flip-flop into DSB17, as it shifts the DSB register. The shift pulse also resets the DSBS flip-flop. If the data bit read from the drum is 0, the DSBS flip-flop remains reset and the shift pulse shifts a 0 into the DSB17 flip-flop. Data transfers continue in this manner until the original 1 bit that was in DSBS is shifted into DSBF.

As the 1 is shifted into the DSBF flip-flop, the DSBF¹ signal sets the OVERFLOW flip-flop (-10:C4). The 18 bits read from the drum are in the DSB register. The next phase B (19th ϕ_B) pulse, enabled by READ and OVERFLOW¹ (-10:D1), generates TAKE WORD which generates DSBINI COND (-10:D3). The DSBINI COND signal checks parity (explained later under Parity Check), and prepares the circuits to read the next word from drum. If SC=SA, the TAKE WORD signal (-9:D1) generates DF DSB1 \rightarrow DF which transfers the DSB contents into the DF register; also TAKE WORD sets the RQ flip-flop (-11:B2/3). The phase B (19th ϕ_B) pulse resets the OVERFLOW flip-flop and the OVERFLOW⁰ signal (enabled by ACT, -8:B4) advances the count of the sector counter.

When the RQ flip-flop is set, the word read from the drum is in the DF register. The RQ signal initiates a computer data break cycle to transfer the DF register contents into the memory location specified by the DCL register (refer to Table 2-2).

Data transfer continues in this manner until all words of the addressed sector have been read. As the 300- μ sec gap is encountered, clock pulses cease to occur and the DONE/START multivibrator reverts to the DONE state. The DONE signal sets the FLAG state. The trailing edge of the ACT signal (-7:D2) generates DT+1 which advances the count of the DT and SA register; this permits the next sector (or track) to be read if continuous sector transfers are specified by the computer program.

With the FLAG state set, the program senses the FLAG state to exit from the read routine.

Reading Two Consecutive Sectors

If the program designates consecutive sector transfers, the DRCONT instruction (refer to Table 2-2) is executed to read the next sector. The DRCONT instruction must occur during the 300- μ sec gap following the previous sector transfer.

Parity Check

As a word is read from the drum, the DSBS¹ signal complements the R PARITY flip-flop (-10:C4). The R PARITY flip-flop is initially set. Since odd parity is generated during the write cycle, the R PARITY flip-flop should be in a reset state after the 18-bit word plus the parity bit are read from the drum. If not, the DSBINI COND+1 μ sec pulse sets the PE flip-flop to indicate a parity error.

DATA ERROR AND PARITY ERROR

Parity error detection was explained under Write One Sector. The data error is generated when the computer does not answer a break request before another break request is made. The break request signal sets the ER SYNC flip-flop (-11:B3). The data request answered pulse from the computer clears the request

flip-flop. The next T7C pulse which occurs during a data break resets the ER SYNC flip-flop. If a data break does not occur, the ER SYNC remains set. The next RQ signal is enabled by ER SYNC to set the DE (data error) flip-flop. The status of the DE·PE error signal can be sensed by the execution of the DRSOK instruction (see Table 5-1).

Maintenance Switch Control of PE·DE

In the ON position, the MAINTENANCE ON/OFF switch (-8:C3) applies $PE^0 \cdot DE^0$ to gate C23L, which enables the phase A, phase B, and READ STROBE pulses. Detection of a data error or a parity error inhibits the clock signals so that all data transfer stops and the contents of all registers can be observed to locate the cause of the error. In the OFF position, the equipment functions normally and data errors or parity errors can be detected by the error flag at the end of a sector transfer.

DRUM TRACK SELECTION CIRCUITS

The output of the DT register (engineering drawing -7) is applied to a decoder which consists of two groups of eight 2-input diode gates; one group for the X address and one for the Y address. The eight X address outputs function as a 2-digit octal address, which is further decoded in the drum X select logic. The eight Y address outputs serve a similar function. The final selection of a drum head is performed in the drum X and Y select circuits as shown in engineering drawing -13. There are 32 field lockout switches; each switch inhibits writing on 8 tracks or 4096 words of drum memory (refer to engineering drawing D-24EFG-0-14).

POWER SUPPLY AND DISTRIBUTION

The serial drum operates from a single power source of 115v, 60-cycle, single-phase. Power control and overload protection within the drum is exercised by a Type 832 Power Control (refer to PW-D-24EFG-0-29). Operation of the power control can be controlled by the REMOTE OFF LOCAL switch on the switch panel or by a contact closure provided by the computer. The fast ac output of the power control operates the drum motor, fan motor, and the Type 779 Power Supply. The delayed ac output operates a relay which provides a POWER CLEAR pulse and applies the -20v to the drum X and Y selection circuits. Indicator lights come on immediately with power, but the drum is not up to speed and cannot be used until the READY light comes on.

The Type 779 Power Supply produces the normal module operating voltages of +10 vdc and -15 vdc, and the -20 vdc for the writer and head select switches. The +10 and -15 vdc outputs are connected to each rack of logic through a color-coded connector and a toggle switch at the right side of each rack, as seen from the module side.

Marginal check terminals are provided on these connectors which are connected in common to all racks. Thus an external power supply can be connected to any connector for marginal checking of all racks. The color coding of these connectors from top to bottom is as follows:

Orange, +10 vdc marginal-check supply

Red, +10 vdc internal supply

Black, ground

Blue, -15 vdc internal supply

Green, -15 vdc marginal-check supply

Three single-pole double-throw switches at the end of each rack of logic allow selection of either the normal internal power supply or the external marginal-check power supply. The top switch selects the +10v supply routed to terminal A of all modules in that rack. In the down position the fixed internal +10v supply connected to the red terminal is supplied to the modules, and in the up position the marginal-check voltage supplied to the orange terminal is supplied to terminal A of the modules. The center switch performs the same selection as the top switch for connection of a nominal +10v level to terminal B of all modules. The bottom switch selects the -15v supply to be routed to terminal C of all modules. In the down position the fixed -15v output of the internal power supply, received at the blue terminal, is supplied to the modules, while in the up position the marginal-check voltage, connected to the green terminal, is supplied to terminal C of all modules.

DRUM MECHANICAL DESCRIPTION

Drum Head Mounting Description

The full complement of magnetic heads is mounted on the drum in a series of blocks, with a line of heads in each block, and the gaps coplanar at one surface as shown in the simplified mechanical diagram Figure 2-9. The flat surface serves as the pad or slider of a hydrodynamic bearing, using the boundary layer of air clinging to the rotating drum as a lubricating or self-pressurizing medium. A single thin strip of spring steel connects each magnetic head/bearing pad to the drum frame. The spring steel reed serves as a combined motion pivot, loading spring, and mounting cantilever.

The action of this simple mechanical system places the magnetic head pad in close proximity to the drum surface when the drum is at operating speed as illustrated in Figure 2-10.

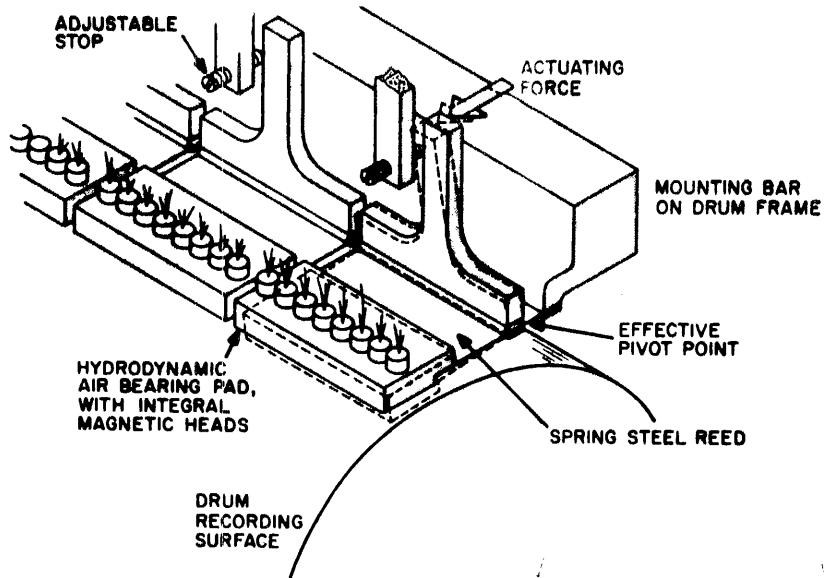


Figure 2-9 Drum Head Mounting

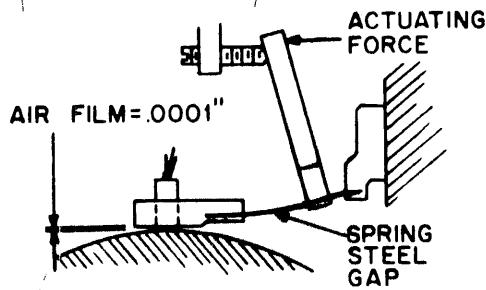


Figure 2-10 Operating Position of Head Pad

Mechanical Actuator

The mechanical actuator moves the heads to close proximity of the drum surface when the drum is up to speed. As the drum comes to speed, a centrifugal switch, mounted on the motor end, closes and sets a time delay relay (red cap). The relay energizes in 1.5 min and sets another time delay relay (yellow cap) which supplies actuating power to the linear motor actuator for 6 sec. After the linear motor pulls the heads in, a holding coil, which is energized from rectified ac, holds in the heads. The 1.5-min delay permits the drum to reach full speed prior to actuation. The 6-sec interval should not be exceeded because the linear motor has a very short duty cycle and can burn out if left energized. A circuit breaker that is thermally actuated by the linear motor current provides further protection for the motor.

Normal shut down of drum power or any power failure will instantly raise the heads. Motor burnout, while not anticipated, results in speed loss so that the centrifugal switch opens and raises the heads.

A fuse mount, located under the right front corner of the cabinet, contains a switch that can be used to actuate the heads. The drum centrifugal switch must be closed to operate this switch.

If the holding coil fails to hold at the end of the pull-in cycle, the manual switch must be opened and closed to restart the cycle.

ANALYSIS OF INSTRUCTIONS

Table 2-1 and Table 2-2 show the analysis of instructions for the write and read cycle, respectively. These tables provide a reference to detailed signal flow during a write or read cycle.

TABLE 2-1 ANALYSIS OF INSTRUCTIONS FOR WRITE CYCLE

Instruction, Operation, or Signal	Function
DRLCWR	Generates IOT 6002 and 6004 pulses which are coupled to the serial drum. MB12=1 to signify a write cycle.
IOT 6002 pulse	Generates DF CLEAR (-9:D1) Generates DCL CLEAR (-4:C1) Generates DDC CLEAR (-11:B1)
DF CLEAR	Clears DF register (-9:B1)
DCL CLEAR	Clears DCL register (-4:B1)
DDC CLEAR	Sets IDLE (-8:B1) Clears RD/WT, RQ, ER SYNC, and DE (-11:B1) Clears OVERFLOW, R PARITY, PAR ERROR, WRITE DATA (-10:C3/4) Clears WRITE ENABLE (-10:D8)
IOT 6004 pulse	Sets RD/WT to WT (write), RQ, and ER SYNC (-11:B2) Transfers AC to DCL (-4:B1)
DATA BREAK CYCLE	Generates DRA (data request answered) and T7 pulse
DRA	Generates DF CLEAR (-9:D1) Generates DCL+1 (-4:C2) which increments DCL Clears RQ (-11:B2)

TABLE 2-1 ANALYSIS OF INSTRUCTIONS FOR WRITE CYCLE (continued)

Instruction, Operation, or Signal	Function
T7 pulse	Clears ER SYNC (-11:C2) Generates DFMB1 → DF (-9:C2) which transfers MB to DF register
DRLBLK	Generates IOT 6104 and IOT 6102 pulse
IOT 6102 pulse	Generates DT CLEAR (-7:D1) which clears DT register Clears DE (-11:B3) Clears PE (-10:C5) Sets IDLE (-8:B1)
IOT 6104 pulse	Transfers AC to DT register (-7:C2) Triggers delay that sets TRA (-8:C1) Generates TAKE WORD
TAKE WORD	Generates DSBINI COND (-10:D3) Sets RQ if WRITE.SC=SA (-11:B2)
DSBINI COND	Generates DSB CLEAR which clears DSB (-10:C2) Generates DSBINI COND+1 (-10:C3)
DSBINI COND+1	Sets R PARITY (-10:C4) Generates DF1 → DSB (-10:C1/2)
DF1 DSB	Transfers DF to DSB (-10:B1) Sets DSBS (-10:B8) Generates ACT+ØB (-10:D3)
DRCONT	Generates IOT 6204 which clears done FLAG and sets TRA (-8:B2), generates TAKE WORD (-10:C1), clears DE (-11:B3) and PER ERROR (-10:C5)

TABLE 2-2 ANALYSIS OF INSTRUCTIONS FOR READ CYCLE

Instruction, Operation, or Signal	Function
DRLCRD	Generates IOT 6002 and 6004 pulses which are coupled to serial drum. MB12=0 to signify a read cycle.
IOT 6002 pulse	Generates DF CLEAR (-9:D1) Generates DCL CLEAR (-4:C1) Generates DDC CLEAR (-11:B1)
DF CLEAR	Clears DF register (-9:B1)
DCL CLEAR	Clears DCL register (-4:B1)
DDC CLEAR	Sets IDLE (-8:B1) Clears RD/WT, RQ, ER SYNC, and DE (-11:B1) Clears OVERFLOW, R PARITY, APR ERROR, WRITE DATA (-10:C3/4) Clears WRITE ENABLE (-10:D8)
IOT 6004 pulse	Transfers AC to DCL (-4:B1)
DRLBLK	Generates IOT 6104 and 6102 pulses
IOT 6102 pulse	Generates DT CLEAR (-7:D1) which clears DT register Clears DE (-11:B3) and PE (-10:C5) Sets IDLE (-8:B1)
IOT 6104	Trigger delay that sets TRA (-8:C1) Transfers AC to DT register (-7:C2) Generates DSBINI COND (-10:D3)
DSBINI COND	Generates DSB CLEAR which clears DSB (-10:C2) Generates DSBINI COND+1 (-10:C3)
DSBINI COND+1	Sets DSB17 (-10:C8) Sets PAR ERROR if parity error occurs during read Sets R PARITY

TABLE 2-2 ANALYSIS OF INSTRUCTIONS FOR READ CYCLE (continued)

Instruction, Operation, or Signal	Function
TAKE WORD	<p>TAKE WORD is generated by the OVERFLOW¹ and READ signal (-10:D1) and performs the following functions:</p> <p>Generates DSB1 DF (if READ·SC=SA) which transfers DSB contents to DF register</p> <p>Generates DSBINI COND (-10:D3)</p> <p>Sets RQ if SC=SA (-11:B2/3)</p>
DATA BREAK CYCLE	Generates DRA (data request answered) and T7
DRA	<p>Generates DCL+1 (-4:C2) which increments DCL</p> <p>Clears RQ (-11:B2)</p>
T7	Clears ER SYNC (-11:C2)
DRCONT	Generates IOT 6204 which clears done FLAG and sets TRA (-8:B2), clears DE (-11:B3) and PAR ERROR (-10:C5)

CHAPTER 3

INTERFACE

All logic signals which pass between the computer and the serial drum are standard DEC levels or standard DEC pulses. A standard DEC level is either ground potential (0.0 to -0.3v) or -3v (-3.0 to -4.0v). Standard DEC pulses are 2.5v in amplitude (2.3 to 3.0v) and are 0.4 μ sec in duration. Positive pulses are referenced to the standard negative level and negative pulses are referenced to ground potential.

Throughout the manual standard DEC ground-potential signals are symbolized by an open diamond (—◇) and standard DEC negative levels are indicated by a solid diamond (—◆). Open and solid arrowheads are used to symbolize standard DEC positive (—▷) and negative pulses (—◁), respectively.

In addition to the logic signal inputs, a contact closure in the computer power control circuit provides the remote turnon signal to the power supply and distribution network in the serial drum. This signal is used to energize or de-energize the serial drum from the computer in normal operation. The effect of this signal can be disabled during maintenance operations to control power application and removal through a switch on the serial drum.

Input signals to the serial drum are listed in Table 3-1, and output signals are listed Table 3-2. The letter and number following the colon indicate the horizontal and vertical coordinates on the engineering drawing where the signal can be found. Signal origins in Table 3-1 and signal destinations in Table 3-2 are given for interface with a PDP-4 computer. Tables 3-3 and 3-4 list the input and output signals, respectively, for the PDP-1. When planning interface between the serial drum and another computer, these tables can be used as a guide for connection to circuit elements performing similar functions. For the PDP-7, refer to Appendix 3 of this manual and the Interface chapter of the PDP-7 Instruction Manual.

Note that input signal levels to the DCL, DFB, DTR, and DDC must be present for at least 3 μ sec before receipt of the IOT pulse or T7B pulse which strobes the data contents into the flip-flops. This delay is required to allow settling of the capacitor-diode gate at the input of each flip-flop.

TABLE 3-1 INPUTS TO 24 FROM PDP-4

Signal Name	Symbol	From PDP-4		To Serial Drum		Function
		Logic	Drawing	Logic	Drawing	
ACB ₁₀ ¹ through ACB ₁₇ ¹	◇	AC (ID)	D-4-00-01-04 D-40004-3	DTR	-7:C	Provides track address to be strobed into DTR by IOT 6104 pulse.
ACB ₂ ¹ through ACB ₁₇ ¹	◇	AC (ID)	D-4-00-01-03 D-4-00-01-04 D-40004-3	DCL	-4:B	Provides initial address of data transfer into DCL.
Begin	→	Keys	D-4-00-C1-01	DDC	-1:B1 -11:B1	Produces DDC CLEAR signal.
Data Request Answered (Equals Data·B·T1) (Data Address \Rightarrow MA)	→	DIC	D-40004-1	DCL DDC DFB	-4:C2 -11:B2 -9:D1	Produces DCL+1 signal which increments DCL. Clears REQUEST (RQ) flip-flop. Produces DF CLEAR signal in write mode.
IOT 6002	→	DS	D-40004-4	DCL DDC DFB	-4:C1 -11:B1 -9:D1	Produces DCL CLEAR signal. Produces DDC CLEAR signal. Produces DF CLEAR signal.
IOT 6004	→	DS	D-40004-4	DCL DDC DSB	-4:B1 -11:B2 -10:C1	Strobes ACB ₂₋₁₇ information into DCL. Strobes MB ₁₂ ¹ into RD/WT, RQ, and DNG flip-flops. Produces TAKE WORD signal if MB ₁₂ is a 1.
IOT 6102	→	DS	D-40004-4	R/WP DCT DTR DDC	-10:C5 -8:B1 -7:C1 -11:B3	OR to clear par error flip-flop. OR to set IDLE to 1. Produces DT CLEAR signal. OR to clear data error (DE) flip-flop.

TABLE 3-1 INPUTS TO 24 FROM PDP-4 (continued)

Signal Name	Symbol	From PDP-4		To Serial Drum		Function
		Logic	Drawing	Logic	Drawing	
IOT 6104	→	DS	D-40004-4	DCT DCT DCT DTR	-10:C1 -10:D3 -8:C1 -7:C2	Produces TAKE WORD signal in write mode. Produces DSB INITIAL CONDITION signal in read mode. Sets transfer request (TRA) to a 1 after 200- μ sec delay. Strobes ACB ₁₀₋₁₇ information into DTR.
IOT 6204	→	DS	D-40004-4	R/WP DDC DCT	-10:C5 -11:B3 -8:B2	OR to clear par error flip-flop. OR to clear data error (DE) flip-flop. OR to set TRA to a 1.
MB ₀ ¹ through MB ₁₇ ¹	◇	MB	D-4-00-01-06	DFB	-9:C	Provides data read from core memory to be written on the drum.
MB ₁₂ ¹	◇	MB	D-4-00-01-06	DDC	-11:B2	Controls setting of RD/WR ¹ , RQ, and ERROR SYNC flip-flops by IOT 6004 pulse.
Remote Turnon	Contact Closure	Power Control		PSD	None	Energizes drum from computer START key.
T7B	→	Timing	D-4-00-01-01	DDC	-11:D3	Produces a T7C pulse which clears the DFB in the read mode, MB → DFB in the write mode, and clears the ERROR SYNC flip-flop in the DDC.

TABLE 3-2 OUTPUTS FROM 24 TO PDP-4

Signal Name	Symbol	From Serial Drum		To PDP-4		Function
		Logic	Drawing	Logic	Drawing	
Data In	→◆	DDC	-11:C2	DIC	D-40004-1	Indicates the direction of data transfers. Data passes into the computer from the drum when this signal is at -3v.
Data Request	→◆	DDC	-11:C2	DIC	D-40004-1	Indicates the serial drum is ready for data transfer.
DCL ₂ ¹ through DCL ₁₇ ¹	→◆	DCL	-4:B	MAR(DIC)	D-4-00-01-05	Holds the core memory address for the next word to be transferred.
DE ⁰ · PE ⁰	→◆	DCT	-8:D3	IOS	D-40004-1	Indicates that no data errors and no parity errors have occurred when at the -3v level.
DFB ₀ ¹ through DFB ₁₇ ¹	→◆	DFB	-10:B	MB(DIC)	D-4-00-01-06	Provides data read from drum which is to be written in core memory.
Transfer Done Flag	→◆	DCT	-8:A4	IOS PIC	D-4004-1	Signals completion of a block transfer when reverting to -3v (Nominally ground level).

TABLE 3-3 INPUTS TO DRUM-1 SERIES FROM PDP-1

Name	Symbol	From PDP-1	To Drum	Function
IO ₁₀ - IO ₁₇	—◇—	IO D-20011	DCL	Provides drum with initial core address
IO ₉ - IO ₁₆	—◇—	IO D-20011	DTR	Provides track address to be strobed into DTR by IOT 0162 pulse
IO ₁₇	—◇—	IO D-20011	Sector Address DTR	Provides sector address to be jammed into SA by X162-7 pulse
START CLEAR	→	General Control D-20007		Produces DDC clear signal
DATA REQ ANSWERED (DRA) TO-HSC BREAK	→	High speed channel D-21303	DCL DDC DFB	Indexes DCL Clears REQ Clears DFB (Write)
TP10	→	General control D-2007	DDC	Forms T10C during break to strobe The MB →DFB (Write)
IOT X161-7	→	DS	DCL DDC DFB	Clears DCL Produces DDC clear Clears DFB
IOT X161-10	→	DS	DCL DDC	Strobes IO →DCL Sets REQ (Write)
IOT 0162-7	→	DS	DT DCT DSB DDC	Jams IO ₁₇ into sector address Produces DT clear Sets idle Clears parity error Clears data error
IOT 0162-10	→	DS	DSB DSB DTR DCT	Produces DSBINI cond Produces TAKE WORD (Write) Strobes IO data into DTR After 200-μsec delay sets TRA

TABLE 3-3 INPUTS TO DRUM-1 SERIES FROM PDP-1 (continued)

Name	Symbol	From PDP-1	To Drum	Function
IOT 162	→	DS	DET DSB DDC	Sets TRA Clears parity error Clears data error
IOT 1163	→	DS	DSB DDC DCT	Clears parity error Clears data error Clears flag and set idle
MB ₀ - MB ₁₇	→	MB	DFB	Provides data from core memory to be written on drum
MB ₈	→	MB	DDC	Controls setting of RD/WT FF by IOT X162-7
REMOTE TURN ON	-15v	Power Supply	836 Power control	Enables drum to energize from remote station

TABLE 3-4 OUTPUTS FROM DRUM-1 SERIES TO PDP-1

Name	Symbol	From Drum	To PDP-1	Function
DATA IN	→	DDC	HSR	Indicates direction of transfer
DATA REQUEST	→	DDC	HSC	Indicates drum is requesting a data break
DCL ₂ ¹ - DCL ₁₇ ¹	→	DCL	HSC	Indicates memory address of next break
DFB ₀ ¹ - DFB ₁₇ ¹	→	DFB	MB	Provides data read from drum which is to be written into core memory
DRUM DONE FLAG	→	DCT	New Logic	Sensed by T. IOT 720163, indicates completion of transfer
DRUM DONE PULSE	→	DCT	SQ BRK	Indicates completion of transfer
PARITY ERROR	→	DSB	New Logic	Sensed by IOT 721164, indicates the presence of a parity error on the last track read
PE ⁰ . DE ⁰	→	DCT	New Logic	Sensed by IOT 720164

CHAPTER 4

INSTALLATION AND OPERATION

SITE REQUIREMENTS

The installation site must provide floor space at least 14 inches wide and 28 inches deep to accommodate the serial drum. At least 9 inches must be provided in front of the cabinet and 15 inches at the back of the cabinet to allow opening of the doors for maintenance.

A source of 115v ($\pm 17\text{v}$), 60 cps, single-phase power must be supplied by the site. This source must be capable of supplying the 8.0-amp starting surge current and 5.0-amp running current required by the serial drum.

Ambient temperature at the installation site can vary between 32 and 105°F (0 to 41°C) without deleterious effect upon equipment operation. For normal operation an ambient temperature range from 70 to 85°F is recommended.

SIGNAL AND POWER CONNECTIONS

All signal connections from the computer to the Type 24 Serial Drum are made at connectors F3 and F4 on the plug panel at the front of the machine. To mate with these connectors, a cable should contain an Amphenol connector of the 115-114P series with a Housing 1391 and Wire Clamp 3057. Maximum signal cable length should not exceed 25 ft. The input and output signals are defined in Tables 3-1 and 3-2 and their wiring connections are given on sheet A-24EFG-0-26.

A grounded, 3-wire power cable is permanently attached to the machine. A standard 3-prong male power plug at the end of this cable allows connection to a power source at least 18 ft from the cabinet.

CONTROLS AND INDICATORS

Toggle switches on the switch panel at the rear of the machine provide all manual control of the serial drum. The function of these switches is as follows:

MAINT ON/OFF

Allows maintenance personnel to select the normal or stop-on-error mode of operation. In the OFF position the equipment functions normally and data errors or parity errors can be detected by the error flag only at the end of a 256-word block. In the ON position detection of data error or parity error by the machine inhibits generation of clock signals (0_A , Read Strobe, and 0_B) so that all data transfer stops and the contents of all registers can be observed to locate the cause of the error.

REMOTE ON/OFF/LOCAL ON	Allows local or remote control of machine energization. In the REMOTE ON position the machine is energized by a contact closure in the computer. The OFF and LOCAL ON positions function as a normal power switch.
FIELD LOCKOUT (0-37)	Each switch allows a group of 16 consecutive address (4096 words) to be inhibited during writing so that the information stored on those tracks cannot be accidentally destroyed.
Visual indication of the machine status and register contents is given on the indicator panel. The functions denoted by these lamps are as follows:	
TRACK ADDRESS (9)	Light to indicate 1's in the drum track address register.
CORE LOCATION (16)	Light to indicate 1's in the drum core location counter.
FINAL BUFFER (18)	Light to indicate 1's in the drum final buffer.
SERIAL BUFFER (18)	Light to indicate 1's in the drum serial buffer.
READY (RD and WR) (2)	Indicate the machine is in either the read or write mode. RD READY light indicates that the initial delay following energization of the power control has elapsed and the machine is ready for use.
TRA	Lights to acknowledge receipt of IOT pulses and indicates that the machine has been taken out of the idle state and is waiting for clock pulses to be read from the drum to assure that the drum is in the correct position before initiating a transfer.
ACT	Lights to indicate that the machine has been taken out of the transfer state and is actively engaged in a data transfer.
FLAG	Lights to indicate that a block transfer has been completed and the machine has been taken out of the active state. The machine remains in this state until the flag is cleared when the machine is set to either the idle or the transfer state.
OVERFLOW	Lights to indicate that a 19-bit word has been assembled in the DSB and is ready for transfer to the DFB in the read mode, or that a 19-bit word has been transferred from the DSB to the drum in the write mode.
REQUEST	Lights to indicate that a data request signal has been sent to the computer to request a data break to transfer a word.

PE

Lights to indicate that the machine has detected a parity error after readin from drum to core. If the MAINT ON/OFF switch is OFF when a parity error occurs, the drum error flag is set to 1; if the switch is ON, the flag is set to 1 and the transfer is terminated.

DE

Lights to indicate that the machine has detected a data error, in that the data request signal from the drum was not answered within the 66- μ sec period required. (When reading a data word is therefore incorrect in the computer core memory or when writing the next word to be written has not been received by the DFB.) If the MAINT ON/OFF switch is OFF when a data error occurs, the drum error flag is set to 1; if the switch is ON, the flag is set to 1 and the transfer is terminated. This condition occurs either because devices with higher priority are connected to the data interrupt control, or because the instruction being executed at the time of the data request takes longer than 66 μ sec for completion.

EQUIPMENT TURNON AND TURNOFF

Operation of the Type 24 can be controlled locally by operation of a switch, or remotely from a signal received from the computer. Control point is selected at the REMOTE ON/OFF/LOCAL ON switch on the switch panel. In normal use this switch is left in the REMOTE ON position with the circuit breaker in the ON position. For maintenance operations this switch is set to the LOCAL ON position to apply power and to the OFF position to remove power. Power is not controlled by manual operation of the circuit breaker. Note that the circuit breaker must be in the ON position to allow either local or remote control of primary power in the serial drum by means of the switch; setting the switch to the REMOTE ON position alone is not sufficient for remote operation.

CHAPTER 5

PROGRAMMING

INSTRUCTION CODES

The instructions that are used with the serial drum are listed in Table 5-1 for the PDP-4 and Table 5-2 for the PDP-1. Similar instructions are used for the PDP-7 (refer to PDP-7 programming documentation).

TABLE 5-1 TYPE 24 SERIAL DRUM INSTRUCTION LIST (PDP-4)

Octal Code	Mnemonic Code	Operation
706006	DRLCRD	Load the drum core location counter with the core memory location information in accumulator bits 2-17. Prepare to read one block of information from the drum into the specified core location.*
706046	DRLCWR	Load the drum core location counter with the core memory location information in accumulator bits 2-17. Prepare to write one block of information into the drum from the specified core location.* Clears all flags.
706101	DRSF	Skip next instruction if the drum transfer done flag is a 1. (The block transfer is complete.)
706102	DRCF	Clear the drum transfer done flag and the $DE^0 \cdot PE^0$ error flag.
706106	DRLBLK	Load the drum track address register with the contents of accumulator bits 10 through 17. Clear the drum transfer done flag, clear the $DE^0 \cdot PE^0$ error flag, and begin a transfer (reading or writing).*
706201	DRSOK	Skip next instruction if the drum transfer done flag is not a 1.
706204	DRCONT	Clear the drum transfer done flag, clear the $DE^0 \cdot PE^0$ error flag and begin a transfer.

*The drum core location counter is incremented after each word transfer and the drum track address register is advanced to the next position at the end of each block transfer if the drum error flag is not set to a 1 and the MAINT ON/OFF switch is in the OFF position.

TABLE 5-2 TYPE 24 SERIAL DRUM INSTRUCTION LIST (PDP-1)

Octal Code	Mnemonic Code	Operation
721161	DWR	Load core location from I/O bits 2-17 to drum control. Set mode to write on drum.
720161	DRD	Load core location from I/O bits 2-17 to drum control. Set mode to read from drum.
720162	DBL	Load drum track address from I/O bits 9-17 and initiate drum transfer. Clears all flags.
721162	DCN	Continue a transfer (do not reset addresses).
720163	DTD	Drum transfer done. Execute the next instruction if the transfer has not been completed; skip the next instruction if the transfer is completed.
720164	DSE	Execute the next command if <u>any</u> error flag exists after a transfer is complete. Skip the next instruction if no error flag exists after a transfer is complete. (Error flags are reset with a drum transfer begin command).
721164	DSP	Execute the next command if the parity flag is on. Skip the next command if the parity flag is off.

DRUM FORMAT AND PROGRAM TIMING

Chapter 2 explained the drum format and showed diagrams of the drum format and word format. A sector transfer begins when the continuously rotating drum reaches the index mark, 1.7 μ sec before the beginning of the data in a selected track and sector. A 300- μ sec interval separates the end of the last sector from the beginning of the first sector on each track.

Because the selection of the track read-write read requires 200 μ sec stabilization time, for continuous transferring a new track must be specified during the first 100 μ sec of the 300- μ sec interval. If selected tracks and sectors are consecutive, uninterrupted transferring may be programmed merely by specifying continuation since the sector and/or track number and core memory location are automatically incremented. However, if a data timing or parity error occurs, the track and sector number are not advanced and operations stop at the conclusion of the sector transfer. This feature allows the program to sense for error conditions and to locate the track and sector at which transmission fails. In general, the continuation command can be given any time within 200 μ sec after the completion flag is set.

The drum completion flag is set upon completion of a sector transfer, causing a program interrupt. The flag is cleared either by a clear flag (DRCF) or automatically when one of two transfer instructions (DRLBLK, DRCONT) is given.

The error flag, which should be checked at the completion of each transfer, indicates either of the following conditions:

1. A parity error has been detected after reading from drum to core memory.
2. The data break request signal from the drum was not answered within the required 66- μ sec period. This condition occurs either because other devices with higher priority are connected to the data break facility, or because an instruction requiring longer than 66 μ sec for completion was in progress when the break request was made. Thus, in reading from the drum, the data word stored in core memory is incorrect; in writing on the drum, the next word has not been received from the computer.

PROGRAMMING SUBROUTINES

The following program examples indicate the operation of the drum system in multiple sector transfers. The subroutines are for the PDP-4; however, similar routines exist for the PDP-1. For the PDP-7, in similar routines the LAW instructions are changed to LAC (see PDP-7 programming documentation). The explanation of example A is explained following its listing. Example B is a more sophisticated routine in which frequent error checks are made; this example will not be explained.

Program Sequence Example A

/SUBROUTINE TO READ OR WRITE n BLOCKS.

/CORE LOCATION A, DRUM BLOCK LOCATION B.

/CALLING SEQUENCE:

/	LAW A	
/	JMS DRUMRD	/OR DRUMWR
/	LAW B	
/	LAM -n+1	/BLOCK NUMBER
DRUMRD,	0	/READ ENTRY
	DRLCRD	/GIVE READ COMMAND
	LAC DRUMRD	/SETUP TO USE COMMON
	DCA DRUMWR	
	JMP COMMON	
DRUMWR,	0	/WRITE ENTRY

	DRLCWR	
COMMON,	XCT I DRUMWR	/FETCH BLOCK NUMBER, LOAD
	DRLBLK	/BEGIN FIRST BLOCK TRANSFER
	ISZ DRUMWR	
	XCT I DRUMWR	/GET NUMBER OF BLOCKS
	DAC TEMP	
DRCON,	DRSF	/WAIT TILL TRANSFER IS DONE
	JMP DRCON	
	DRSOK	/CHECK FOR VALID TRANSFER
	HLT	/STOP IF NOT GOOD
	ISZ TEMP	/INDEX BLOCK NUMBER
	JMP .+2	
	JMP DRDONE	
	DRCONT	/GIVE CONTINUE FOR MORE BLOCKS
	JMP DRCON	
DRDONE,	DRCF	
	ISZ DRUMWR	/ADVANCE RETURN
	JMP I DRUMWR	

/END OF DRUM READ OR WRITE SUBROUTINE

The LAW A instruction loads the accumulator with the address of the initial core memory location which contains the first word of the sector transfer. The JMS DRUMWR jumps to the write entry point and deposits the contents of the program counter +1 (which addresses the LAW B instruction) into the DRUMWR location. Note that the accumulator, which contains the core memory address, remains unchanged; therefore, the next instruction (DRLCWR) can transfer the accumulator contents which contain the core memory address into the drum core memory address register (DCL register). The next instruction is an execute instruction (XCT I) indirectly addressed to DRUMWR. Since the DRUMWR location contains the address of the LAW B instruction, the LAW B instruction is executed, loading the accumulator with the track address. The DRLBLK is then executed to transfer the accumulator contents, which contain the track address, into the drum track register and start the sector transfer. Data transfer begins between the drum and core memory; data is transferred automatically (without further intervention by the program); each word transfer takes the word in core memory specified by the drum memory address and writes it on the specified track and sector. Following a word transfer, the drum memory address is incremented so that the next transfer takes the word from the next sequential memory location.

The ISZ DRUMWR instruction increments the contents of the DRUMWR location so that the DRUMWR location contains the address of the next sequential instruction (following LAW B) which is the LAM -n+1 instruction. The LAM -n+1 instruction specifies the number of block transfers in 2's complement form. The XCT I DRUMWR instruction loads the accumulator with the number of block transfers; the DAC TEMP stores the number of block transfers into location TEMP.

The DRSF (skip if transfer done) senses the status of the drum FLAG and if the sector transfer is complete, the program skips to the DRSOK instruction; if not, the program loops back to the DRSF instruction and continues in this loop until the sector transfer is complete.

The DRSOK instruction (skip if no error) senses the error flag for errors occurring during the previous sector transfer. If an error occurs, the next instruction is executed which halts the program. If no error occurs, the program skips to the ISZ TEMP instruction. The ISZ TEMP instruction senses the TEMP location for all 0's which signifies that the block transfer is complete. If not 0, the block transfer is not complete; therefore, the TEMP location is incremented and the next instruction (JMP +.2) is performed. The JMP +.2 (jump to this location +2) advances the program to DRCONT which initiates another block (sector) transfer. The JMP DRCON instruction returns the program back to the DRSF instruction to wait till the sector transfer is complete.

When the block transfer is complete, the ISZ TEMP instruction senses a 0 in TEMP; consequently, the next instruction is performed which jumps the program to DRDONE. The DRCF instruction clears all flags in the drum. The ISZ DRUMWR instruction increments the DRUMWR location so that it will address the advance return location. This permits the JMP I DRUMWR to return the program control to the main program.

Program Sequence Example B

/DRUM SUBROUTINES

/A = INITIAL CORE MEMORY ADDRESS B = INITIAL DRUM ADDRESS

/CALLING SEQUENCE:	LAC (A)	/OR LAW (A)
/	JMS DRUMRD OR DRUMWR	
/	LAW B	/OR LAC (B)
/	LAM -n+1	/n = NO. OF BLOCKS TO WRITE
/	JMP SUBR	/RETURN TO DRSUB +1, FOR /MULTIPROGRAMMING
/	JMP ERR	

DRLCRD = 706006

DRLCWR = 706046

DRLBLK = 706106

DRCONT = 706204

DRSF = 706101

DRSOK = 706201

DRCF = 706102

DRUMWR,

0

DRLCWR

/DRUM WRITE

DAC DRUMT1

LAC DRUMWR

DAC DRUMRD

JMP DRUMCM

DRUMRD,

0

DRLCRD

/DRUM READ

DAC DRUMT1

DRUMCM,

XCT I DRUMRD

DAC DRUMT2

DRLBLK

/START TRANSFER

ISZ DRUMRD

XCT I DRUMRD

/BLOCK COUNTER

DAC DRUMT3

ISZ DRUMDR

LAC I DRUMDR

DAC DRSUB

ISZ DRUMRD

/POINTS TO ERROR RETURN

JMP DRSUB

DRCN,

DRCONT

ISZ DRUMT2

LAC DRUMT1

ADD DECIMAL (256) OCTAL

DAC DRUMT1

DRSUB,

0

DRSF

JMP .-1

DRSOK

JMP DREXIT

ISZ DRUMT3

	JMP DRCON	
	ISZ DRUMRD	
DREXIT,	DRCF	
	JMP I DRUMRD	
DRUMT1,	0	/CURRENT CORE ADDRESS
DRUMT2,	0	/DRUM ADDRESS
DRUMT3,	0	/COUNTER
START		

FIELD LOCKOUT SWITCHES

The programmer should be aware of the settings of the FIELD LOCKOUT switches to avoid attempting to write at track addresses which are inhibited by switches in the up position. The octal addresses inhibited by each switch are as follows:

<u>Switch</u>	<u>Addresses</u>	<u>Switch</u>	<u>Addresses</u>
0	0000 to 0017	20	0400 to 0417
1	0020 to 0037	21	0420 to 0437
2	0040 to 0057	22	0440 to 0457
3	0060 to 0077	23	0460 to 0477
4	0100 to 0117	24	0500 to 0517
5	0120 to 0137	25	0520 to 0537
6	0140 to 0157	26	0540 to 0557
7	0160 to 0177	27	0560 to 0577
10	0200 to 0217	30	0600 to 0617
11	0220 to 0237	31	0620 to 0637
12	0240 to 0257	32	0640 to 0657
13	0260 to 0277	33	0660 to 0677
14	0300 to 0317	34	0700 to 0717
15	0320 to 0337	35	0720 to 0737
16	0340 to 0357	36	0740 to 0757
17	0360 to 0377	37	0760 to 0777

CHAPTER 6

MAINTENANCE

The maintenance techniques for the serial drum consist of the normal maintenance and troubleshooting techniques employed on digital equipment; these techniques include visual inspections, cleaning air filters, fault isolation, etc. Any techniques peculiar to the 24 Serial Drum are described in this chapter.

ADJUSTMENTS

Timing Checks and Adjustments

Using the oscilloscope and referring to engineering drawing -8, check the timing of the Type 4303 Integrating Single Shot at location 1C9, and the Type 1304 Delay at location 1D24. If necessary, adjust the timing of these modules by turning the potentiometer screw which is accessible through a hole in the handle.

Check the single-shot by observing the 1 output at 1C9W while triggering the oscilloscope on 1C9K. During each revolution of the drum the single shot is triggered every 1.7 μ sec for approximately 17 msec during data reading and receives no pulses during the 300- μ sec gap. The output at terminal 1C9W should be at ground level during the gap, drop to -3v at the first triggering pulse, and remain at -3v until 3.4 μ sec after the last triggering pulse is received before reverting to ground potential.

Check the timing of the 1304 Delay module (1D24) by observing the negative read strobe pulse at terminal 1D24E while triggering the oscilloscope on the \emptyset A pulse. Read strobe pulses should follow \emptyset A pulses by approximately 0.3 μ sec. Observe the read strobe pulses and the amplified output of a magnetic read head by connecting the second input of the dual-trace oscilloscope to terminal 1E24S. It is important that the read strobe pulses occur at the negative peak of the sinusoidal read signal. Measurements should be made using several different head outputs, and the read strobe pulse should be adjusted for an average of the measurements to eliminate large differences in peak playback time.

Drum Sense Amplifier Check and Adjustment

The Type 1537 Drum Sense Amplifier modules at locations 1E25 (clock track) and 1E24 (data track) are checked for proper slice or threshold level at terminal S. This measurement can be made with the oscilloscope by measuring the amount the base line shifts above ground when the signal is connected to the input. The clock track sense amplifier slice level should be +100 mv. The data track sense amplifier slice level should be +150 mv. Adjustment of the slice level can be achieved by turning the potentiometer screw which is accessible through a hole in the module handle.

Drum Head Mounting Adjustments

Adjustment of the magnetic heads is provided by the stop screw for each pad of heads and its actuating arm, as shown in Figure 6-1.

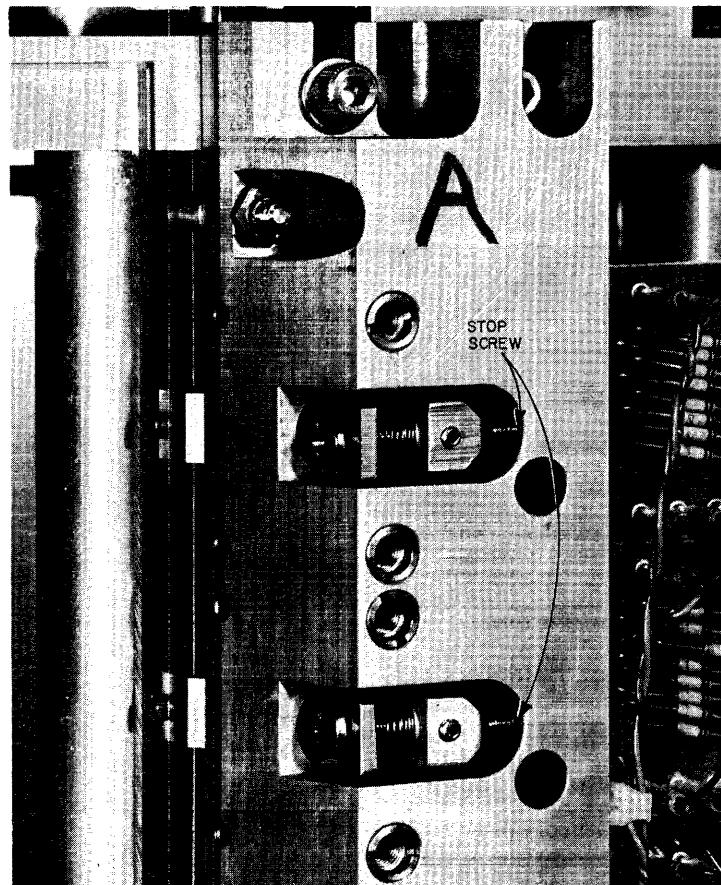


Figure 6-1 Stop Screw Position

With this stop screw properly positioned, the actuating arm moves the pad to a position where the read is slightly bent and the pad is tangent to the drum surface at the line of head gap. These adjustments are made at the factory and ordinarily need not be changed, at least no more than a minor adjustment. However, should adjustment be necessary, proceed as follows:

1. Connect an oscilloscope to 1E25S to observe the preamplifier output for the drum head in question.

2. Set the DTA to address the drum head in question. Engineering drawing -13 shows the bar and pad location and the octal address of each drum head.
3. Set the drum control status to read.
4. Using a 5/64 hexagonal for socket heads, adjust the stop screws until a maximum output is noted on the oscilloscope as shown in Figure 6-2. The adjustment screw is located on the right side of each bar viewing the drum as shown in Figure 6-1.

CAUTION

If head adjustment is attempted with diode boards in place, make sure that the adjustment wrench is placed, and/or insulated to prevent shorting connections or components to ground.

The best method of making this check is to run a program in which the patterns of all 0's, all 1's, or alternate 1's and 0's are written on the selected track, then read the data and monitor the output of the selected track. If data on the selected track is to be retained, it should be read into core memory before proceeding with this adjustment. Rewrite the selected track and read the recorded signal after every adjustment.

Pad Leveling Adjustment

The amplitude of head playback signals among the eight heads in each pad is set as uniformly as possible by using the pad leveling screws which are accessible at the outer surface of each bar, roughly adjacent to the upper and lower edges of each pad. This may be checked on heads 1 and 8 (top and bottom heads) with secondary reference to heads 2 and 7. Clockwise rotation of a pad leveling screw tends to increase signal amplitude at that end of the pad. Continuously write and read the selected heads, always alternating between the two.

MARGINAL CHECKS

Marginal checks are performed to aggravate borderline conditions within the logic to reveal observable faults. The checks are performed by operating the equipment logic circuits from an external, adjustable power source, such as the DEC Type 734 Variable Power Supply. (See Chapter 2, Power Supply and Distributions for descriptions of marginal check terminals and switches.)

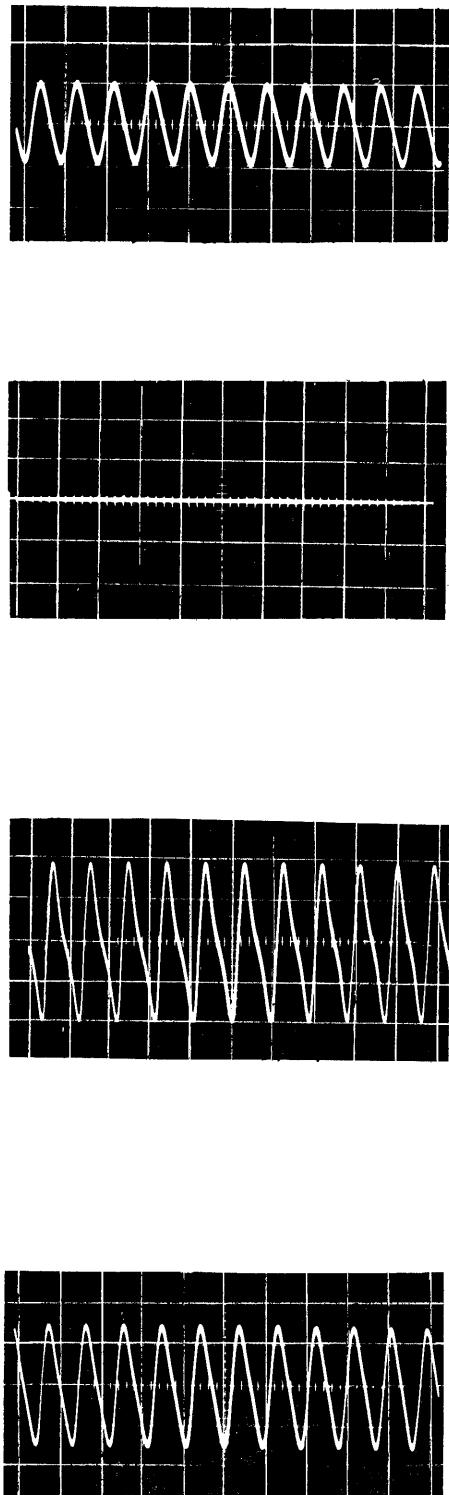
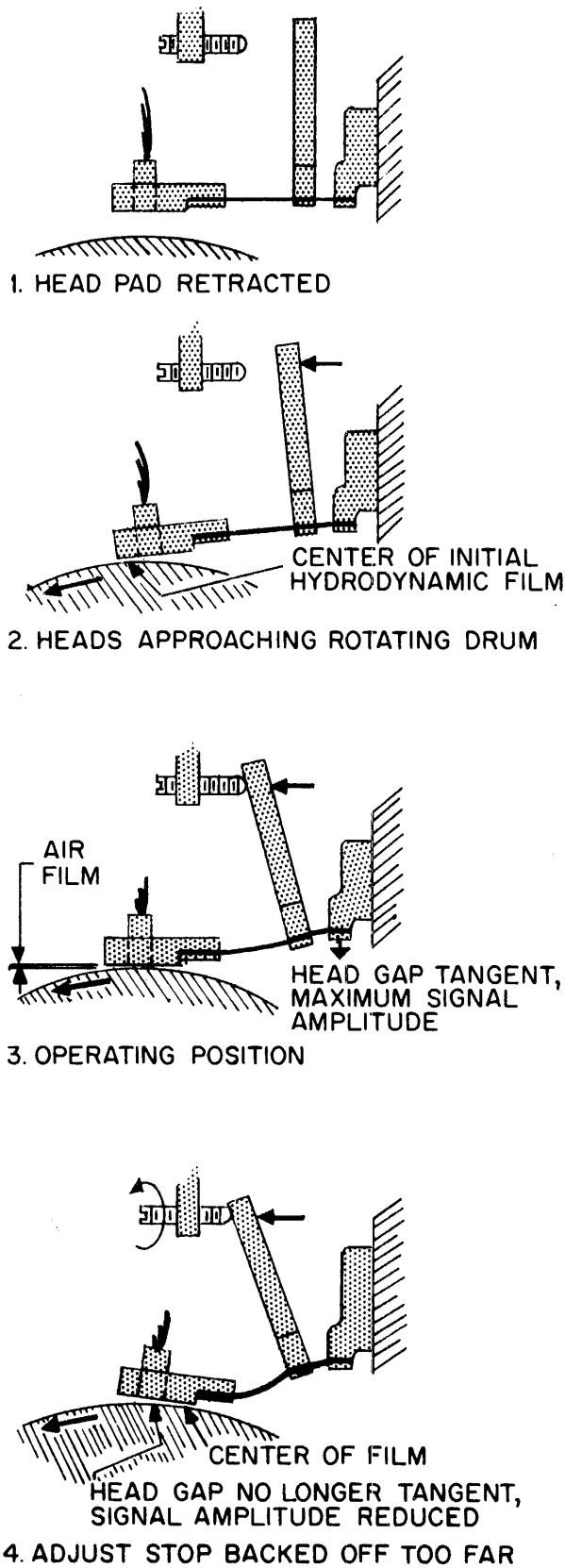


Figure 6-2 Operating Positions of Head Pad

Raising the bias voltage above +10 is equivalent to lowering the amount of base drive on a particular transistor. This in turn simulates a lower gain driving transistor. Raising the bias voltage thus tends to indicate low gain transistors. Lowering the bias voltage below +10v simulates a condition where the voltage drop across the previous driving transistor (V_{CE}) has increased; this tends to indicate high V_{CE} drop (leakage) transistors or low gain driving transistors. The -15v supply margins are not checked in the serial drum because raising or lowering the -15v does not affect the majority of control logic, since it is the collector load voltage and is usually clamped to -3v. The +10v margin should be about $\pm 5v$.*

By recording the level of bias voltage at which circuits fail, progressive deterioration can be plotted and expected failure dates predicted. Therefore, these checks provide a means of planned replacement. Marginal checks of the +10 (A) supply (top switch at the left of the rack) to rack E varies the slice level on the drum sense amplifier modules and so is a valuable tool in verifying the capability of the machine to read and write on the drum surface. Normally increasing the +10 (A) supply by 5 or 6v also increases the slice level and causes bits to be dropped out. Decreasing the +10 (A) source by 5 or 6v usually lowers the slice level and causes bits to be picked up.

To perform marginal checks, proceed as follows:

1. Connect the external marginal-check power supply to the colored connector on any rack between the green (+) and the black (ground) terminal.
2. Energize the marginal-check power supply and adjust the outputs to supply the nominal +10 vdc.
3. Start equipment operation in a repetitive pattern or in a routine which fully utilizes the circuits in the rack to be tested.
4. Set the top switch on the rack to be checked to the up position.
5. Lower the +10v marginal-check power supply until normal system operation is interrupted. Record the marginal-check voltage. At this point marginal transistors can be located and replaced.
6. Start equipment operation. Then decrease the +10v marginal-check supply until normal operation is interrupted, at which point record the marginal-check voltage. Transistors can again be replaced.

*The 1537 Sense Amplifier, 1C1 and 1E25, has only $\pm 2v$ margins on +10B.

7. Stop operation and return the top switch to the down position.
8. Repeat steps 2 through 7 for the center switch on the logic rack being checked.
9. Repeat steps 2 through 8 for each rack of logic to be checked.
10. De-energize and/or disconnect the external marginal-check power supply.

DIAGNOSTICS

The diagnostic program is a test procedure designed to check the basic control functions performed by the machine and to determine the reliability of recording on various tracks. Specifically the program performs the following:

1. Writing and checking of any desired pattern on the entire drum, writing one track at a time.
2. Writing and checking of specific patterns on the entire drum, writing one track at a time.
3. Writing and checking of random numbers over the entire drum, writing four tracks at a time.

Prepare a perforated tape or other vehicle for loading the following program into the computer.

24/

WRA = 2000

RDA = 4000

BEGIN,	LAC DLNGTH
	CMA
	ADD (1)
	DAC DLOOP1+3
	DAC DWRITE+1
	ADD (3)
	DAC D3A
D0,	LAS
	SMA
	JMP D1
	HLT

LAS
 JMS DLOOP1
 JMP D0
D1, LAM TB-TBE
 DAC T2
 LAW TB-1
 DAC 17
D2, LAC I 17
 JMS DLOOP1
 ISZ T2
 JMP D2
D3, LAC (736425) /TEST RANDOM 2000 WD PATTERNS
 DAC RNK
 LAC (NOP)
 DAC DRSUB+4
D3A, LAM /MODIFIED, -DLNGTH+4
 DCA T1
 DZM DK1
D4, LAM -17777
 DAC T2
 LAW WRA-1
 DAC 10
D5, JMS RN
 DAC I 10
 ISZ T2
 JMP D5
D6, LAC (WRA)
 JMS DRUMWR
 LAC DK1
 LAM -3
 JMP DRSUB+1
 JMP WZE
D7, JMS DCMP
 LAM -3
 LAM -1777
 ISZ DK1

ISZ T1
JMP D4
JMP D3A
DCMP,
0 /COMPARE READ AREA AGAINST WRITE AREA
LAC (RDA)
JMS DRUMRD
LAC DK1
XCT I DCMP
JMP DRSUB+1
JMP .+1
ISZ DCMP
XCT I DCMP
DAC DCT1
LAC (LAC WRA-1)
DAC 10
LAC (LAC RDA-1)
DAC 11
DCMP2,
LAC I 10
SAD I 11
JMP .+2
JMS DCMPE
ISZ DCT1
JMP DCMP2
ISZ DCMP
JMP I DCMP
DCT1,
0
DK1,
0
DK2,
0
DK3,
0
DCMPE,
0 /TYPE OUT DRUM ERROR
TIN
LAC DK1
DAC DK2 /CHANNEL NO.
LAC (LAC RDA)
CMA
ADD 11

DCMPE1, ADD (DECIMAL, 255 OCTAL)
SPA
JMP DCMPE2
ADD (-1)
ISZ DK2
JMP DCMPE1
DCMPE2, ADD (DECIMAL, 255 OCTAL)
SPA
CMA
DAC DK3 /WORD NO.
LAC DK2 /TRACK NUMBER
TWORDZ
6
TAB
LAC DK3 /WORD NUMBER
TWORDZ
6
TAB
XCT 10 /WORD WRITTEN
TWORD
6
TSP
XCT 11 /WORD READ
TWORD
6
JMP I DCMPE
DLOOP1, 0 /DO WRITING AND CHECKING
JMS DSPRD
JMS DWRITE
LAM /MODIFIED, -DLNGTH+1
DAC T1
DZM WRA
DZM DK1
DLOOP2, JMS DCMP
LAM
LAM DECIMAL, 255 OCTAL

	ISZ DK1	
	ISZ WRA	
	ISZ T1	
	JMP DLOOP2	
	JMP I DLOOP1	
T1,	0	
T2,	0	
DSPRD,	0	/SPREADS 256 WORDS IN WRA
	DAC DSPRDA	
	LAM DECIMAL, 255 OCTAL	
	DAC DSPRDC	
	LAW WRA-1	
	DAC 10	
	LAC DSPRDA	
	DAC I 10	
	ISZ DSPRDC	
	JMP .-2	
	DZM WRA	
	DZM DK1	
	JMP I DSprd	
DSPRDC,	0	
DSPRDA,	0	/WRITES ALL CHANNELS
DWRITE,	0	
	LAM	/MODIFIED, -DLNGTH+1
	DAC DWC	
	LAC (JMP DREXIT)	
	DAC DRSub+4	
DW1,	LAC (WRA)	
	JMS DRUMWR	
	LAC DK1	
	LAM	
	JMP DRSub+1	
	JMS WZE	
	ISZ WRA	
	ISZ DK1	
	ISZ DWC	

DCMPE1, ADD (DECIMAL, 255 OCTAL)
SPA
JMP DCMPE2
ADD (-1)
ISZ DK2
JMP DCMPE1

DCMPE2, ADD (DECIMAL, 255 OCTAL)
SPA
CMA
DAC DK3 /WORD NO.
LAC DK2 /TRACK NUMBER
TWORDZ
6
TAB
LAC DK3 /WORD NUMBER
TWORDZ
6
TAB
XCT 10 /WORD WRITTEN
TWORD
6
TSP
XCT 11 /WORD READ
TWORD
6
JMP I DCMPE

DLOOP1, 0 /DO WRITING AND CHECKING
JMS DSPRD
JMS DWRITE
LAM /MODIFIED, -DLNGTH+1
DAC T1
DZM WRA
DZM DK1

DLOOP2, JMS DCMP
LAM
LAM DECIMAL, 255 OCTAL

	ISZ DK1
	ISZ WRA
	ISZ T1
	JMP DLOOP2
	JMP I DLOOP1
T1,	0
T2,	0
DSPRD,	0 /SPREADS 256 WORDS IN WRA
	DAC DSPRDA
	LAM DECIMAL, 255 OCTAL
	DAC DSPRDC
	LAW WRA-1
	DAC 10
	LAC DSPRDA
	DAC I 10
	ISZ DSPRDC
	JMP .-2
	DZM WRA
	DZM DK1
	JMP I DSPRD
DSPRDC,	0
DSPRDA,	0 /WRITES ALL CHANNELS
DWRITE,	0
	LAM /MODIFIED, -DLNGTH+1
	DAC DWC
	LAC (JMP DREXIT)
	DAC DRSUB+4
DW1,	LAC (WRA)
	JMS DRUMWR
	LAC DK1
	LAM
	JMP DRSUB+1
	JMS WZE
	ISZ WRA
	ISZ DK1
	ISZ DWC

	JMP DW1	
	JMP I DWRITE	
DWC,	0	
RN,	0	/RANDOM NUMBER GENERATOR
	LAC RNK	
	CLL V RAR	
	SZL	
	XOR (400000)	
	XOR (335671)	
	ADD (335671)	
	DAC RNK	
	JMP I RN	
RNK,	0	/WORKING NUMBER
WZE,	0	
	TIN	
	LAC DK1	
	TWORDZ	
	6	
	TSP	
	LAC (FLEX WRE)	
	TY3	
	JMP I WZE	
TB,	0	
	777777	
	525252	
	252525	
	666666	
TBE,	111111	
DLNGTH,	400	/256 TRACKS DECIMAL
START		

This program assumes that DEC Readin Mode Loader program and standard teleprinter subroutines are stored in core memory. If the subroutines are not in the computer, prepare routines as listed in Appendix 1, or equivalent, and load them into the computer.

To use this program set the ADDRESS switches to 7770, load the tape in the reader, and depress the START key. When the program is in the computer press the STOP key, set the ADDRESS switches to 24, then press the START key.

Phase a - If bit 0 of the ACCUMULATOR switches is a 1, the program will halt. Put the pattern desired to be written on the drum in the ACCUMULATOR switches and press CONTINUE. The pattern will be written on all tracks and checked. Note that during this phase and during phase b below, the first word written on each track is the track number.

After the entire drum (tracks $0-127_{10}$ or $0-255_{10}$) has been checked, the program will continue with phase b unless bit 0 of the ACCUMULATOR switches is a 1, in which case the machine will halt again and the entire process can be repeated. The switches can be changed any time after CONTINUE is pressed.

If bit 0 of the ACCUMULATOR switches is a 0 when starting the program, phase b will begin immediately.

Phase b - During this phase the following patterns are written and checked over the entire drum, writing one track at a time:

000000
777777
525252
666666
111111

(The first word on each track will be the track number)

Phase c - When phase b is completed, the program will generate pseudo-random numbers and write and check the entire drum writing and reading, four tracks at a time (i.e. 0-3, 1-4, 2-5, 3-6 etc. through $124-127_{10}$ or $252-255_{10}$). This phase will continue indefinitely until the machine is stopped.

If information is misread from the drum, the following typical message will be typed, and the program will continue checking the next channel:

000100 000236 525252 525250

Where: word one = the track number (octal 0-255)

word two = word number (octal 0-377)

word three = the word written on the drum

word four = the word read from the drum (in this example bit 16 was dropped)

If an error occurs during writing, the message 000100 WRE will be typed, indicating a write error on track 100 (octal). The program will continue; however, if this error occurs during phase c, start the program over manually. Normally this error cannot occur, as parity is not checked during writing, and no timing problems are imposed by the programming.

The program has been assembled for a 256_{10} track drum. To use the same program for a 128_{10} track drum, change register DLNGTH to 200_8 . $DLNGTH = 313$ (memory location).

Head Pad Replacement

This replacement should be preformed only by qualified personnel. To replace the head pads, the following tools are required:

1. Surface plate (at least 3 ft by 2 ft)
2. Two 2-inch machinist's parallels
3. Aligning pin, VRC (Vermont Research Corp.) part no. 59P7
4. Steel scale, 1/32-inch calibrations
5. Height comparator with 0.000050 inch calibration (or finer), with less than 5 gram contact pressure. The "Electroprobe" manufactured by Federal Products, Providence, R.I., is suggested.
6. Adjustable height gage, 3 to 4 inch micrometer caliper

Replacement of the head pad must be done with the head mounting bar removed from the drum. This is done by removing the four socket head cap screws at the ends of the bar, disconnecting the matrix wiring, and setting the head mounting bar on the two parallels on the surface plate. Place the bar with the bearing surface of the pads upward, and the stop adjusting screws accessible at the edge of the surface plate.

Remove the head pad by removing screws at the pad and those holding the leads with a strain relief and the associated connector. Insert the new pad, bending the leads gently. Replace all screws. Check polarization of connector locating pins (which also serve as mounting screws) to ensure proper mating with other half. Before tightening head pad mounting screws, insert aligning pin through corresponding hole in bar and up into aligning hole in the loose pad.

Insert aligning pin into pad carefully making sure that no leads are caught at the pin hole. With the pin in place, scale the distance from each end of the pad to the reed mount and adjust the parallel within 1/64 inch. Tighten pad mounting screws and recheck parallelism. Remove the aligning pin and proceed to height adjustment.

Using housing flat-to-drum dimensions and the required drop allowance, measure the thickness of the bar and parallels in use and calculate the height setting for the height gage as follows:

HOUSING-TO-DRUM DIMENSION - DROP ALLOWANCE = REQUIRED BAR-TO-HEAD DIM

REQUIRED BAR-TO-HEAD PAD DIM + PARALLEL THICKNESS + BAR THICKNESS =
HEIGHT GAGE SETTING

Set the height gage to size using the micrometer caliper; then use the height gage to set the comparator to zero or center range. Rotate the actuator link and allow the head pad to move into actuated position. Using a hexagonal wrench in the corresponding stop screw, lower the pad being adjusted until the height comparator reads approximately zero at the center of the pad. Check elevation of the entire pad. Using the two differential pad leveling screws between the reed mount and bar, and the stop screw for over all elevation, set the pad level within 0.0001 inch (leading to trailing edge) and 0.0002 inch (end to end).

CHAPTER 7

ENGINEERING DRAWINGS

This chapter contains reduced copies of the block schematics, circuit schematics, and other engineering drawings necessary for understanding and maintaining this equipment. Only those drawings which are essential and are not available in the referenced pertinent documents are included. Refer to the table of contents for a list of these drawings.

A complete set of engineering drawings is supplied with the equipment. Should any discrepancy exist between the drawings in this chapter and those supplied, the assumption is that the latter drawings are correct.

DRAWING NUMBERS

Engineering drawing numbers contain five pieces of information, separated by hyphens. This information consists of a 2-letter code specifying the type of drawing; a 1-letter code specifying the size of the drawing; and variable-length codes specifying the type number of the equipment, the manufacturing series of the equipment, and a serial number for the drawing. The drawing type codes are:

- BS, block schematic or logic diagram
- CD, cable diagram
- CS, circuit schematic
- FD, flow diagram
- PW, power wiring
- RS, replacement schematic
- TD, timing diagram
- UML, utilization module list
- WD, wiring diagram

CIRCUIT SYMBOLS

The block schematics of Digital equipment are multipurpose drawings that combine signal flow, logical function, circuit type and location, wiring, and other pertinent information. Individual circuits are shown in block or semiblock form, using special symbols that define the circuit operation. These symbols are similar to those in the Digital System Modules Catalog but are often simplified. Figure 7-1 illustrates most of the symbols used in Digital engineering drawings.

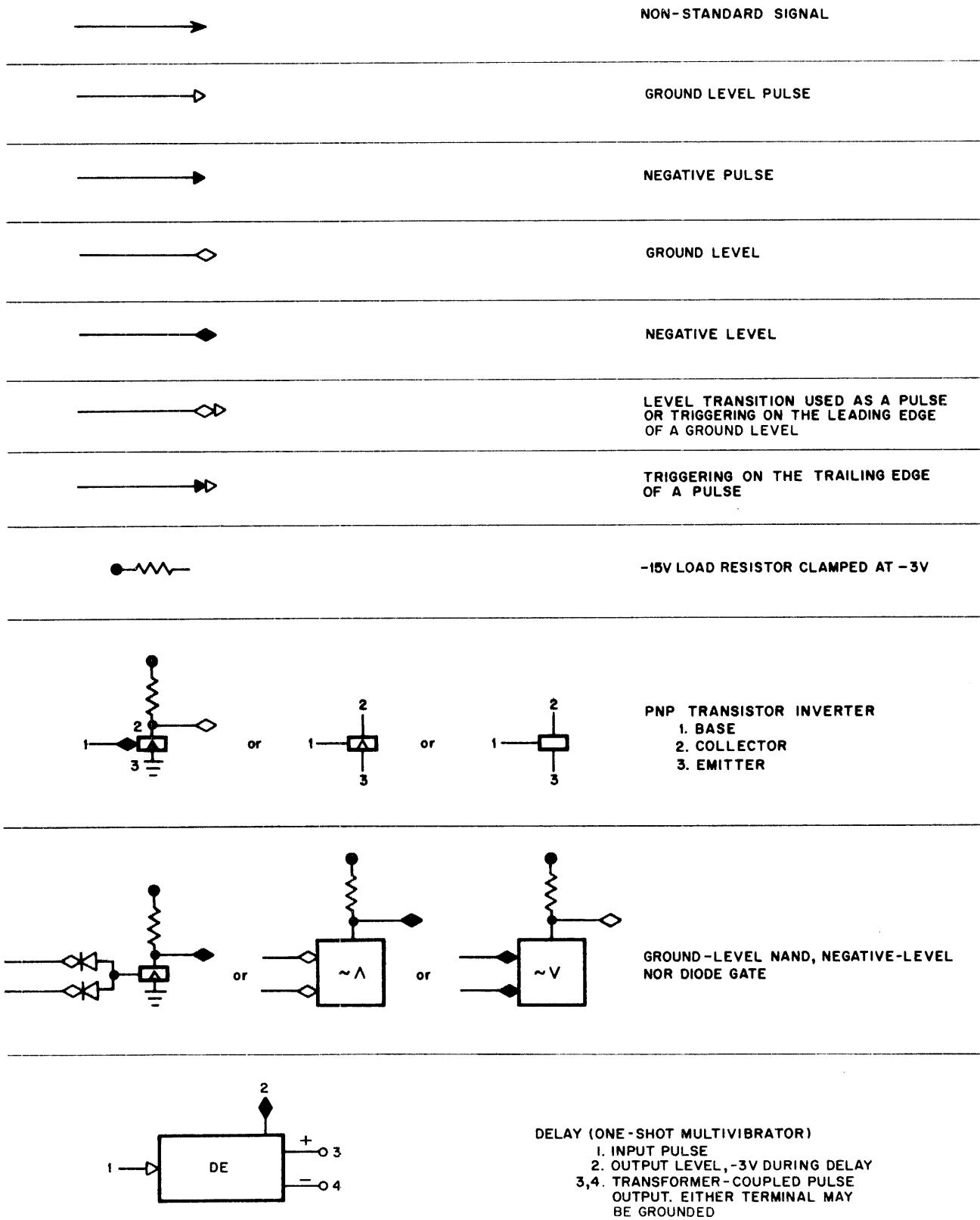
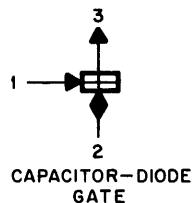
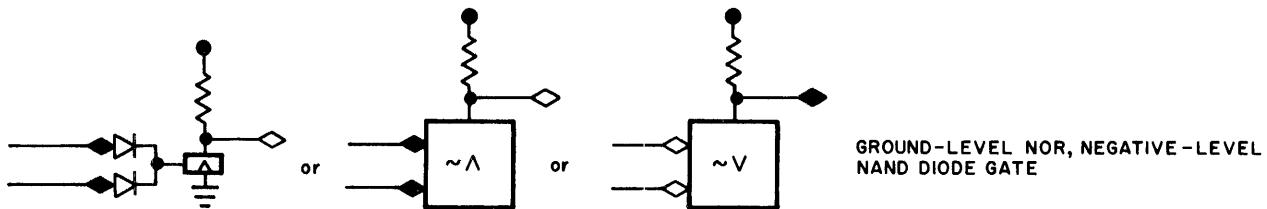


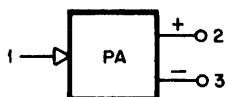
Figure 7-1 DEC Logic Symbols



1. PULSE INPUT
2. CONDITIONING LEVEL INPUT
3. PULSE OUTPUT

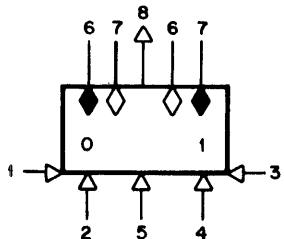


PULSE INVERTER



PULSE AMPLIFIER

1. PULSE INPUT, POLARITY INDICATED
BY INPUT SIGNAL
2,3. TRANSFORMER-COUPLED PULSE
OUTPUT, EITHER TERMINAL MAY
BE GROUNDED



FLIP-FLOP (MOST FLIP-FLOPS HAVE ONLY SOME
OF THE FOLLOWING):

1. DIRECT-CLEAR INPUT
2. GATED-CLEAR INPUT
3. DIRECT-SET INPUT
4. GATED-SET INPUT
5. COMPLEMENT INPUT
6. OUTPUT LEVEL, -3V IF 0, 0V IF 1
7. OUTPUT LEVEL, 0V IF 0, -3V IF 1
8. CARRY PULSE OUTPUT, UPON BEING CLEARED

Figure 7-1 DEC Logic Symbols (continued)

LOGIC SIGNAL SYMBOLS

A Digital logic signal symbol is shown at the input of almost all circuit symbols to specify the assertive conditions required to produce a desired output.

All logic signals are either standard Digital logic levels or standard Digital pulses. A standard Digital logic '0' is either a ground (0 to -0.3v) or -3v (-2.5 to -3.5v). Logic signals are generally given mnemonic names which indicate the condition represented by assertion of the signal. An open diamond

(—◇—) indicates that the signal is a level and that ground represents assertion; a solid diamond (—◆—) indicates that the signal is a level and that $-3v$ represents assertion.

The standard Digital negative pulse is indicated by a solid triangle (—►) and goes from ground to -2.5 or $-3v$ (-2.3 to $-3.5v$ tolerances). The standard Digital positive pulse, indicated by an open triangle (—►), goes either from $-3v$ to ground or from ground to $+2.5v$ ($+2.3$ to $+3.0v$). The width of the standard pulses are used in this equipment is either 1.0 , 0.4 , or $0.07 \mu\text{sec}$, depending on the module and application.

Occasionally, the transition of the level is used at an input where a standard pulse is otherwise expected and a composite symbol (—◆►) is drawn to indicate this fact. The triangle is drawn open or solid depending, respectively, on whether the positive ($-3v$ to ground) or the negative (ground to $-3v$) transition triggers circuit action. The shading of the diamond either is the same as that of the triangle to indicate triggering on the leading edge of a level, or is opposite that of the triangle to indicate triggering on the trailing edge. Any other signal is nonstandard and is indicated by an arrowhead (—►) pointing in the direction of signal flow. Figure 7-2 illustrates the use of many of these symbols.

COORDINATE SYSTEM

Each engineering logic drawing is divided into 32 zones (4 horizontal, and 8 vertical) by marginal map coordinates. Figure references in the text are usually followed by a letter and a digit specifying the zone in which the referenced circuit is located.

MODULE IDENTIFICATION

Two numbers appear in or near each circuit symbol or inside the dotted line surrounding multiple circuit symbols. The upper number designates the module type and is usually four digits long. Standard modules are identified by this number in the Digital System Modules or FLIP CHIP Modules Catalog. Nonstandard modules are described in this manual or in the referenced pertinent documents.

The lower number is the module location code. Sometimes this code is just the 1- or 2-digit basic number indicating the module connector location within a mounting panel, as shown in Figure 7-2. Usually this basic number is preceded by a number to identify the cabinet and a letter to indicate the mounting panel within the cabinet. Mounting panels are usually identified alphabetically, with A in the upper location.

Module connector terminals are identified by letters next to the circuit symbol. To identify any particular terminal, the terminal letter is added to the module location as a suffix. These letters run in alphabetical order, with the letters G, I, O, and Q omitted. (See Figure 7-2 for examples.)

Some modules have the suffix "J" or "R" following the normal 4-digit module type number. "J" indicates that some of the jumpers have been removed. An octal code may follow the module number to indicate which jumpers are connected, but in general the block schematic must be consulted. "R" indicates that all the output collectors have clamped load resistors jumpered to them. A number and suffix such as 4112-70R" indicates that the first three outputs (H, L, and P), counting octally in alphabetical order, have clamped load resistor jumpers and that the last three outputs (T, W, and Z) do not.

EXAMPLE

Figure 7-2 illustrates Digital symbols and nomenclature. The circuit shown is a Type 4303 Integrating Single Shot used to control the enabling time of several gates. The module is located in the twelfth position from the left (when viewed from the front, or wiring side) of mounting panel B (the second from the top) in cabinet 1, specified by the module location code 1B12. The symbol marked **DELAY** is a monostable multivibrator with two complementary outputs, terminals U and W each shown twice. In the stable state these terminals are at ground and -3v as shown by the diamonds inside the symbol on the left. The -3v from terminal U is the assertive level for a gate in 2D18 and is applied to terminal F as the **SAFE** signal. When the multivibrator is triggered, it momentarily goes to the 1 state and terminals U and W reverse their voltage levels, as shown by the diamonds representing the 1 state conditions. Terminal U now provides a ground assertive level to terminal M of a gate in 1B15, and terminal W provides a -3v assertive level to terminal F of a gate in 1D02. The time the multivibrator remains in the 1 state is a function of the capacitor selected by jumpering terminal D to terminal E and the setting of the external variable resistor between terminals X and Z.

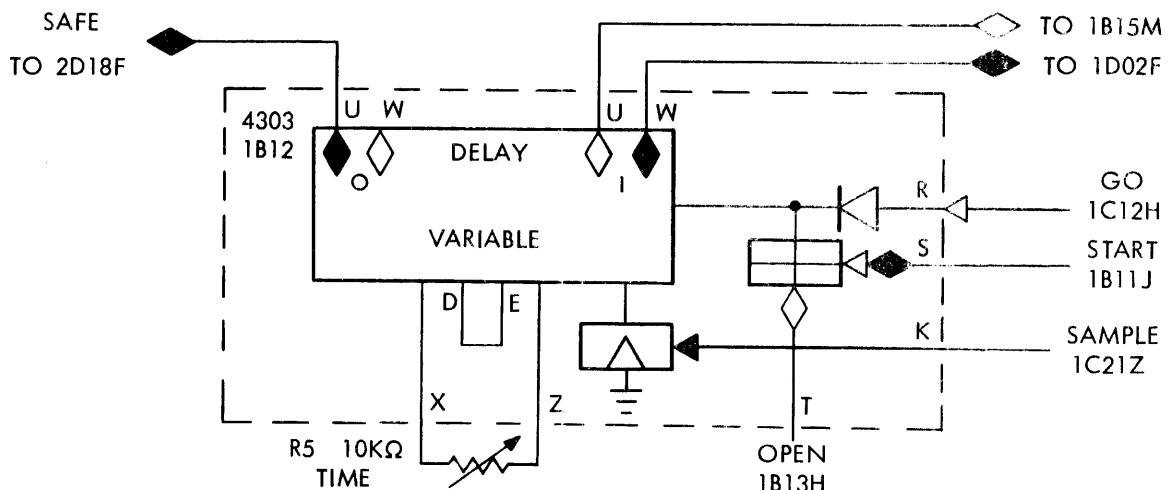


Figure 7-2 Typical Digital Logic Block Diagram

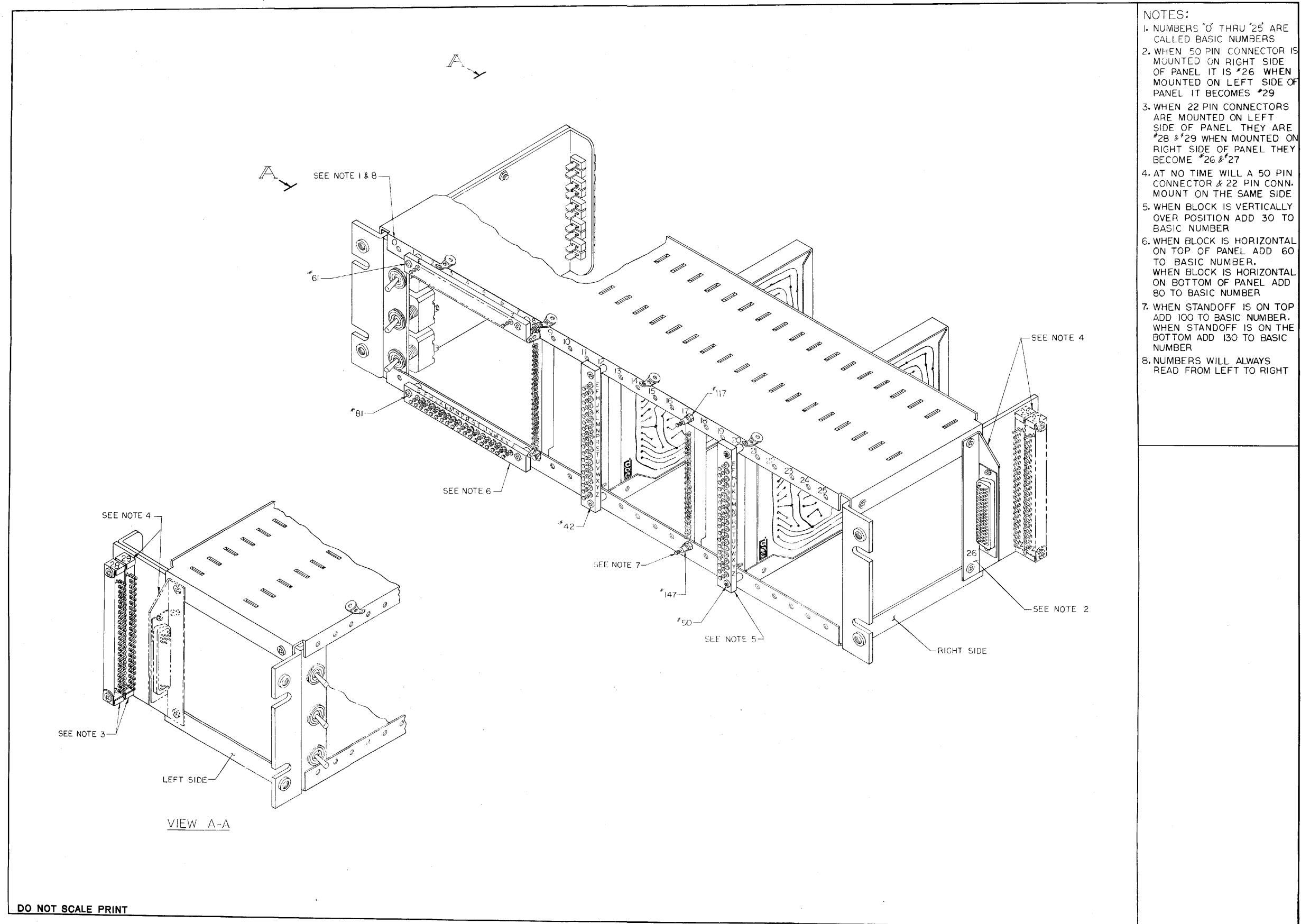
The multivibrator is triggered to the 1 state when any one of three signals occurs. One of these is a positive pulse named GO from a pulse amplifier in 1C12. Another is a negative pulse named SAMPLE from a NOR gate in 1C21, which is applied to the base of an inverter. The third is the positive transition at the trailing edge of the START signal, a negative level from a delay in 1B11. This will only trigger the capacitor-diode gate when a ground signal designated OPEN from a flip-flop in 1B13 has been present for at least 1 μ sec.

SEMICONDUCTOR SUBSTITUTION

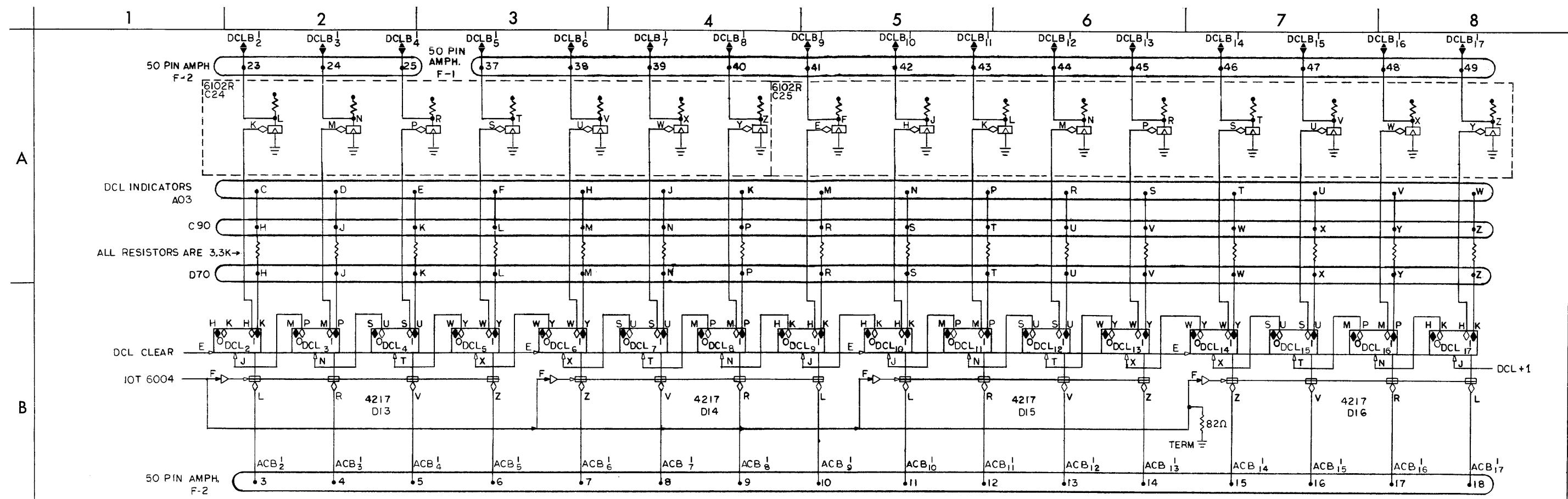
The majority of DEC semiconductors used in modules of the 24 Drum can be replaced with standard EIA components as specified in Table 7-1. Exact replacement is recommended for semiconductors that are not listed.

TABLE 7-1 SEMICONDUCTOR SUBSTITUTION

DEC	EIA	DEC	EIA
D-001	1N276	DEC 1754	2N1499A or 2N1754
D-003	1N994	DEC 3009	2N3009
D-007	1N277	DEC 3639	2N3639
D-662	1N645	MA90	2N2451
D-664	1N914	MD95	2N2489
D-668	Two 1N3606 in Series	MD114	2N1499A
D-670	1N3653	1/4 M6.8 Az 5	1N4099
DEC 999	MM999		



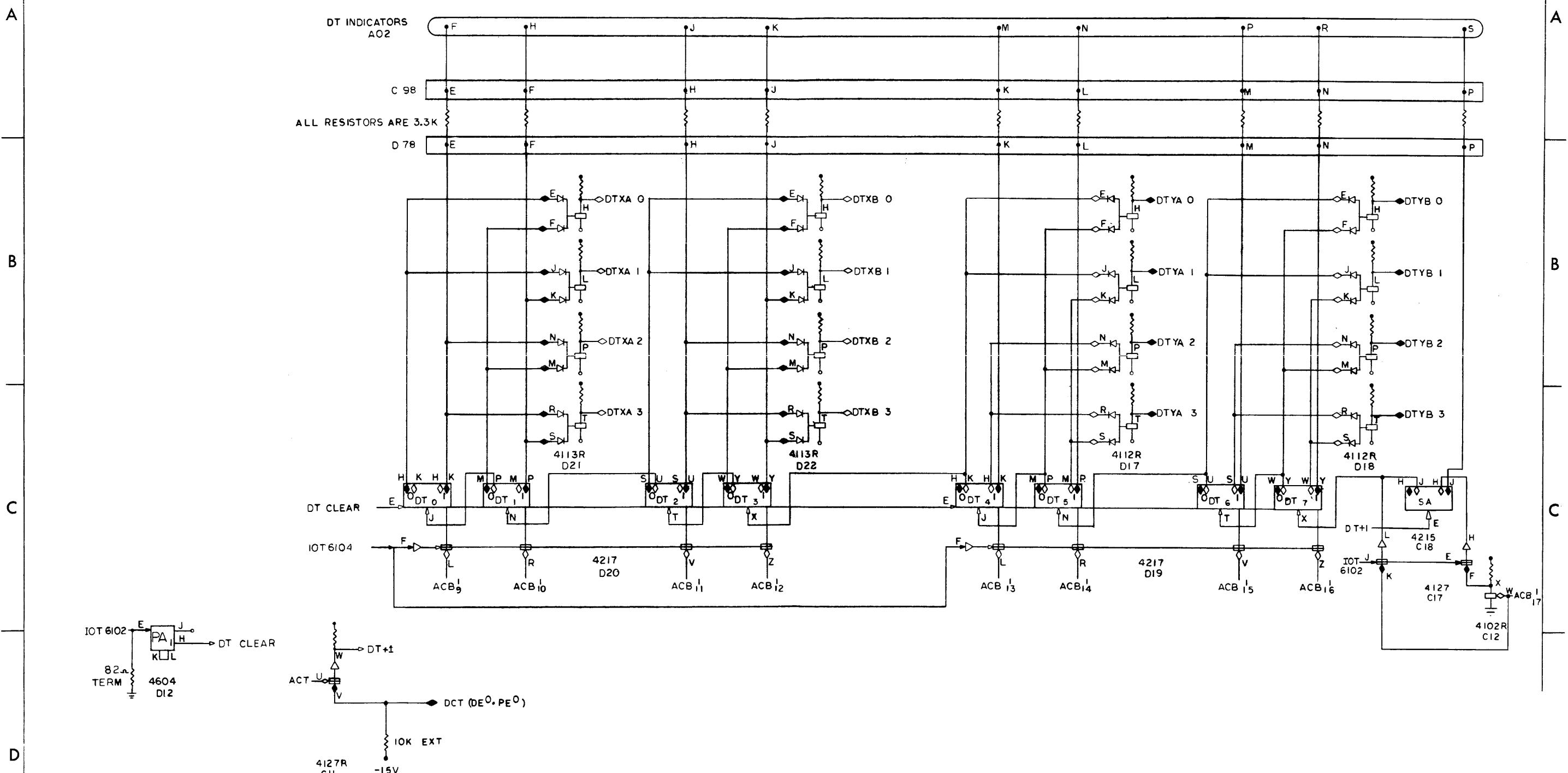
Drum Core Location Counter BS-D-24604

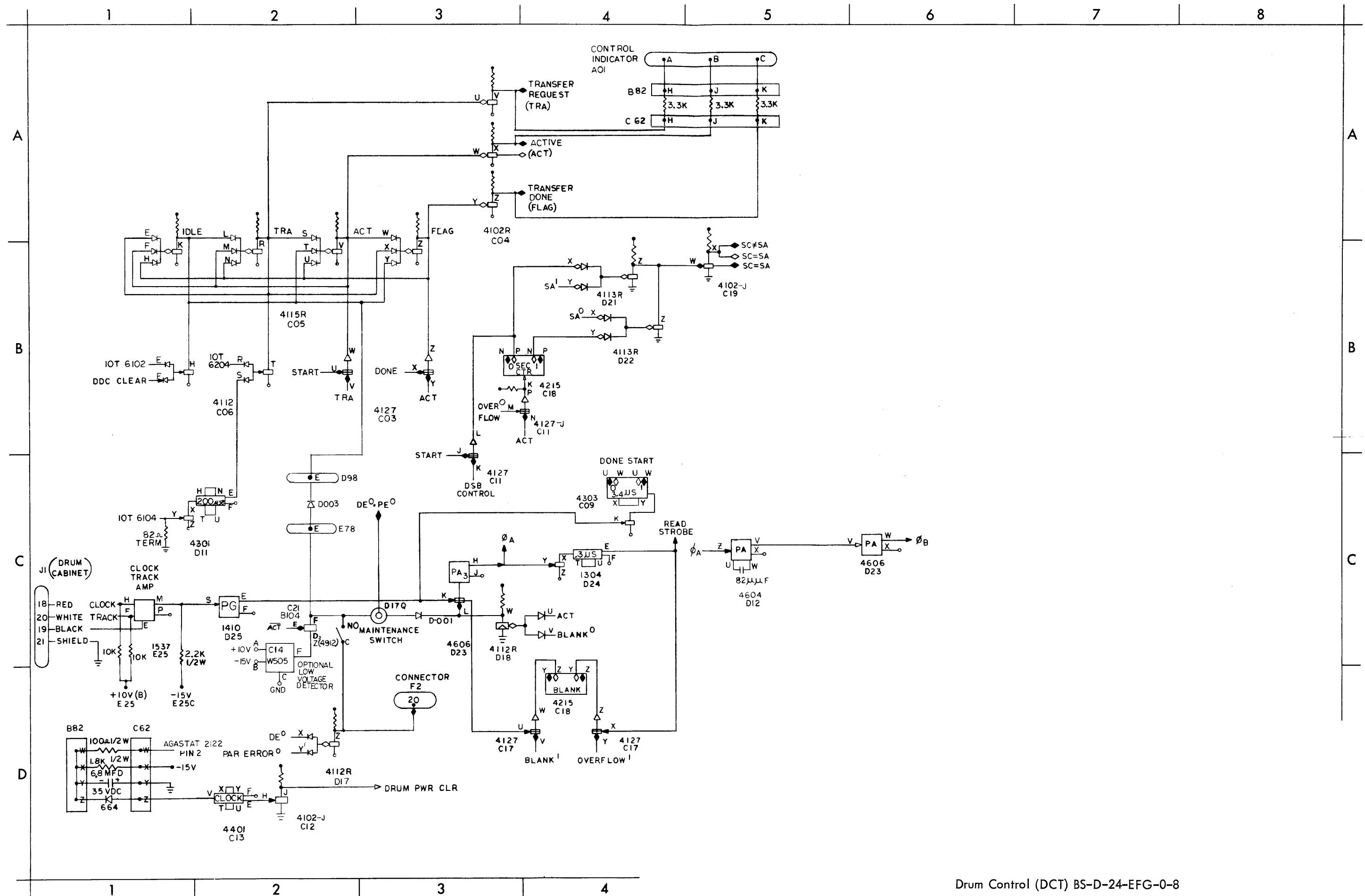


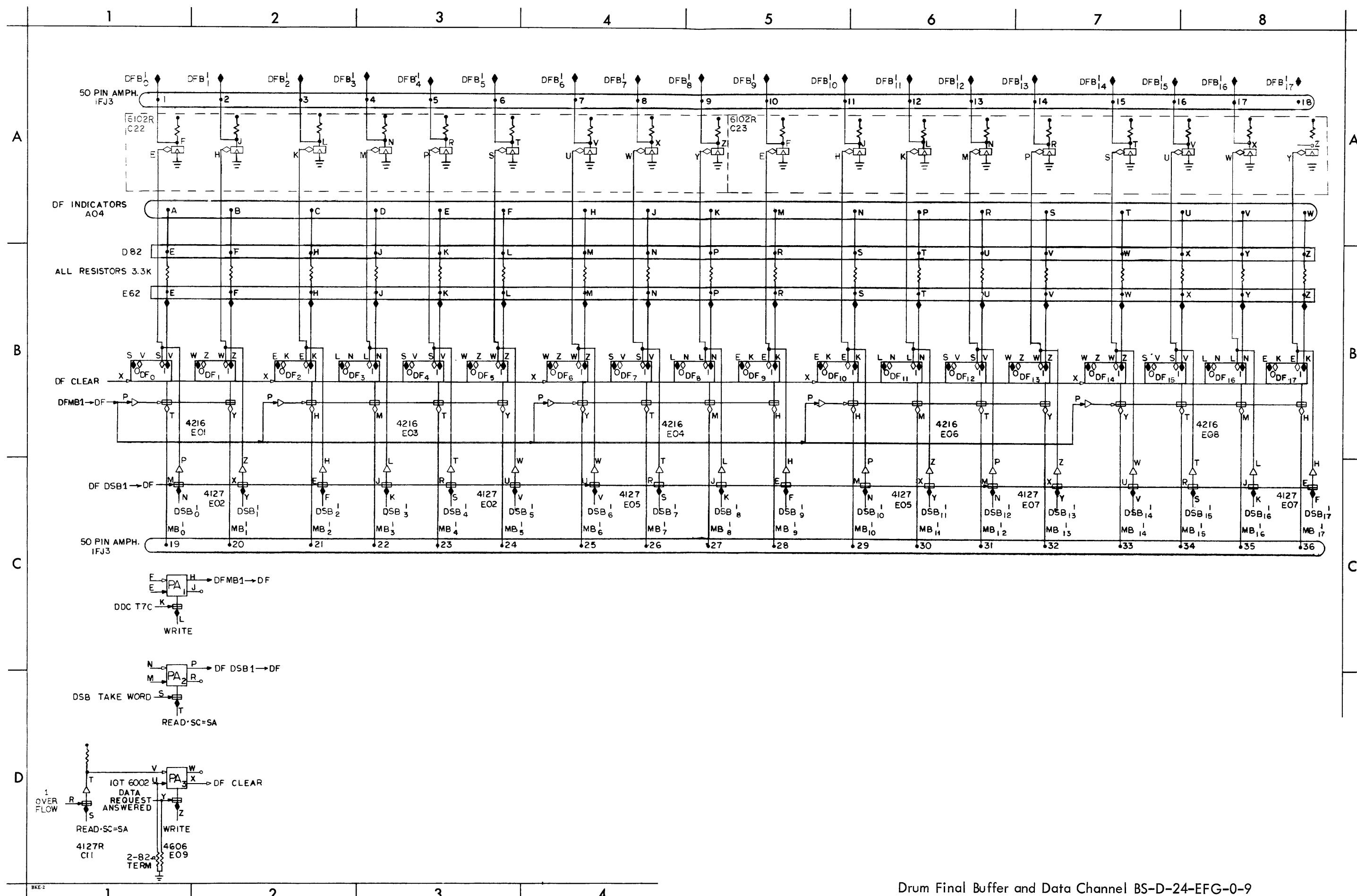
D

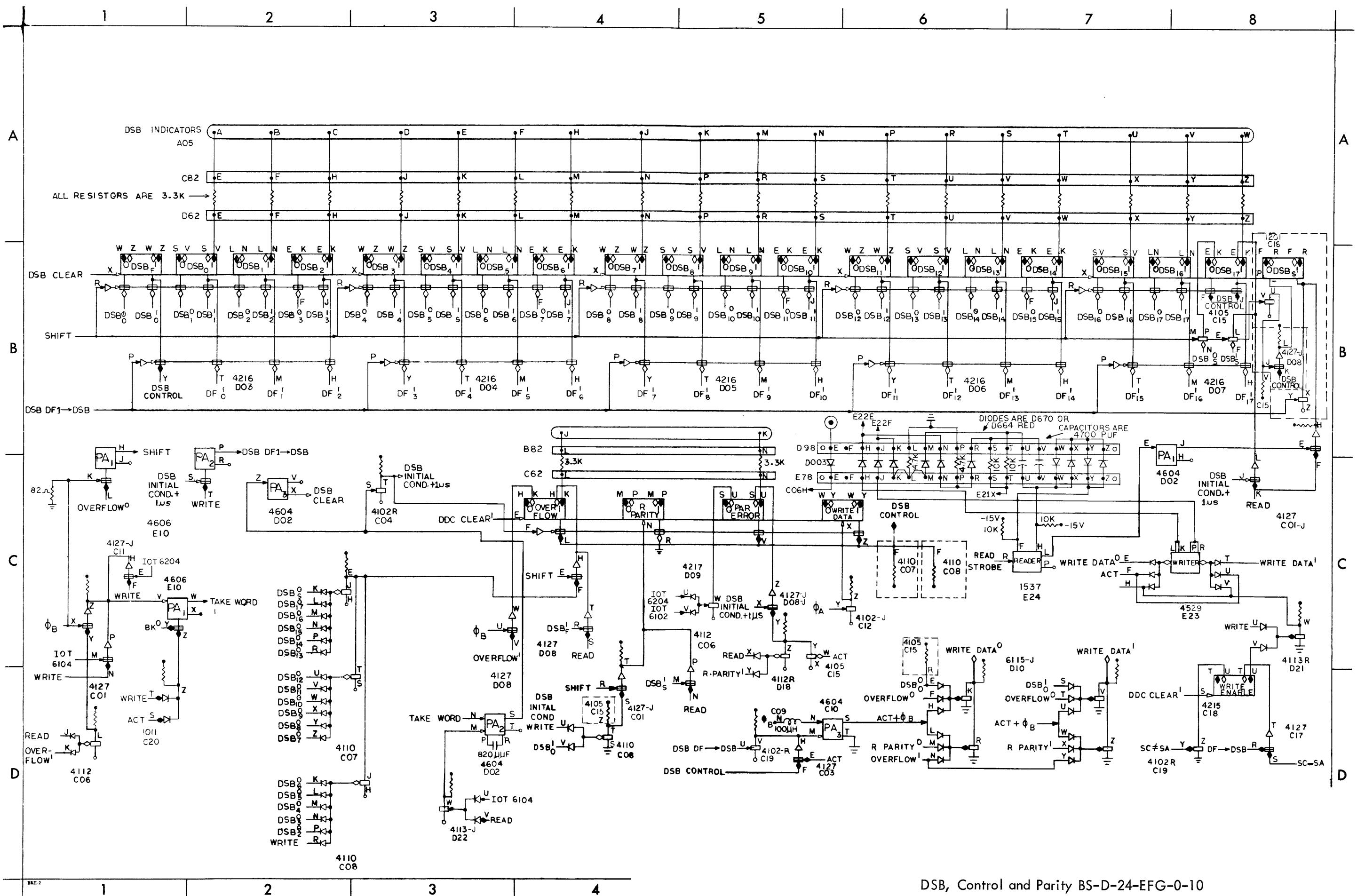
Drum Track Address Register and Decoding (X and Y)
BS-D-24-EFG-0-7

1 | 2 | 3 | 4 | 5 | 6 | 7 | 8



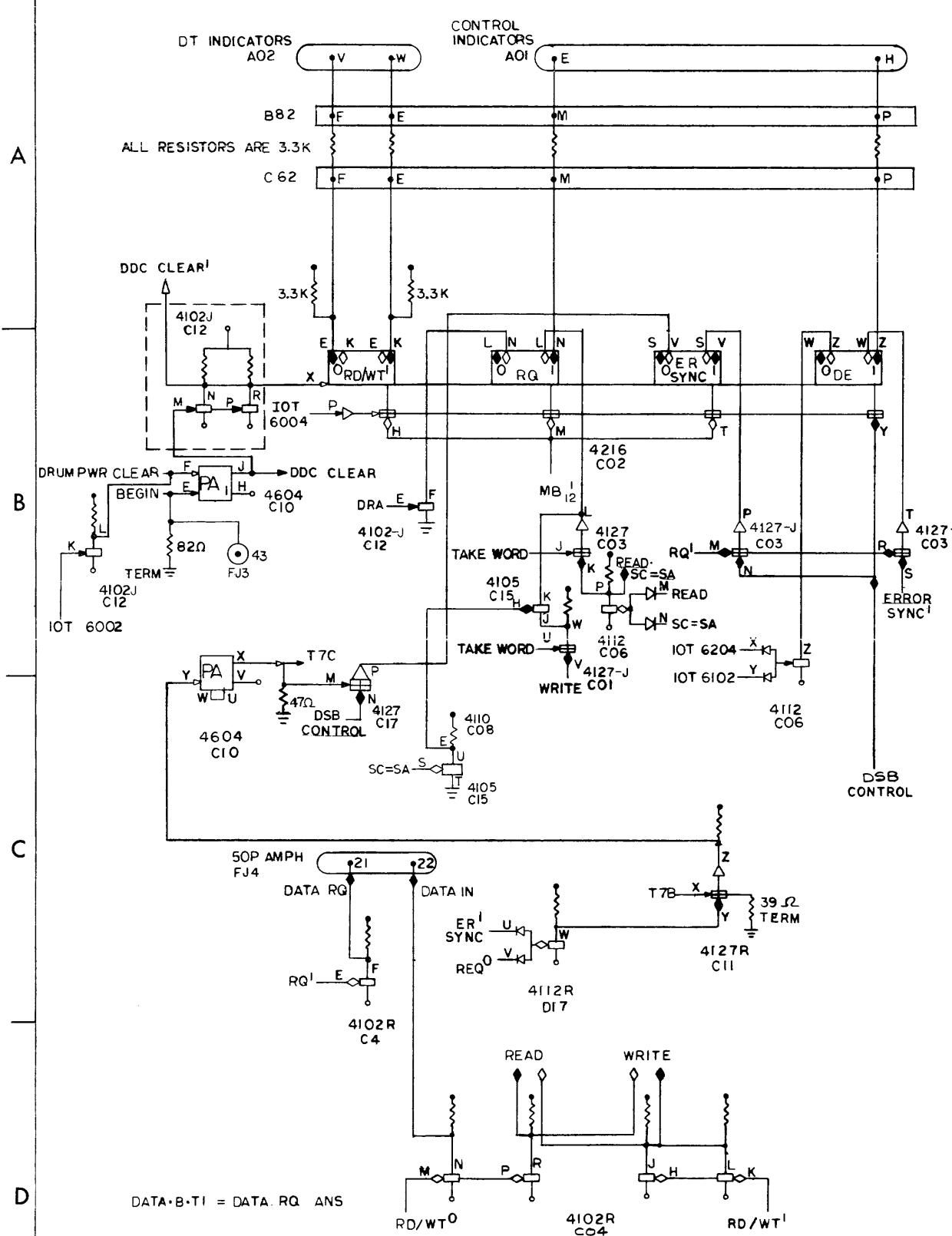






Drum Data Channel (DDC) BS-D-24-EFG-0-11

1 2 3 4 5 6 7 8



Write Field Lock Out Select BS-D-24-EFG-0-14

1 | 2 | 3 | 4 | ↓ | 5 | 6 | 7 | 8

A

B

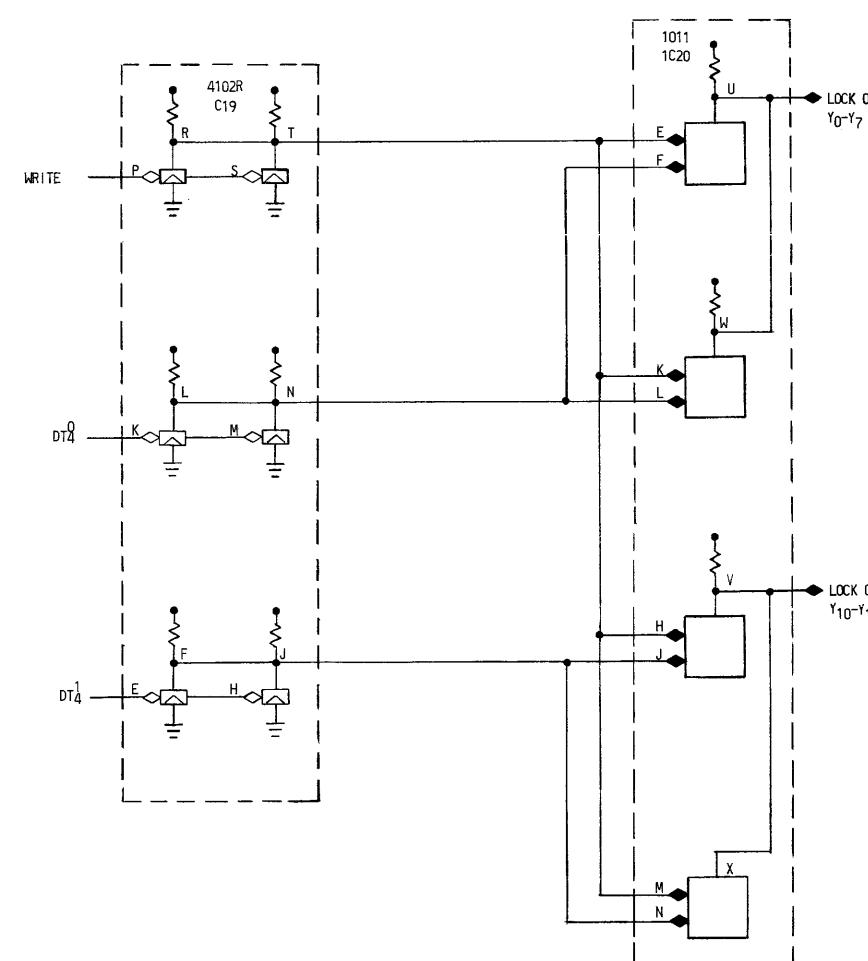
C

D

A

B

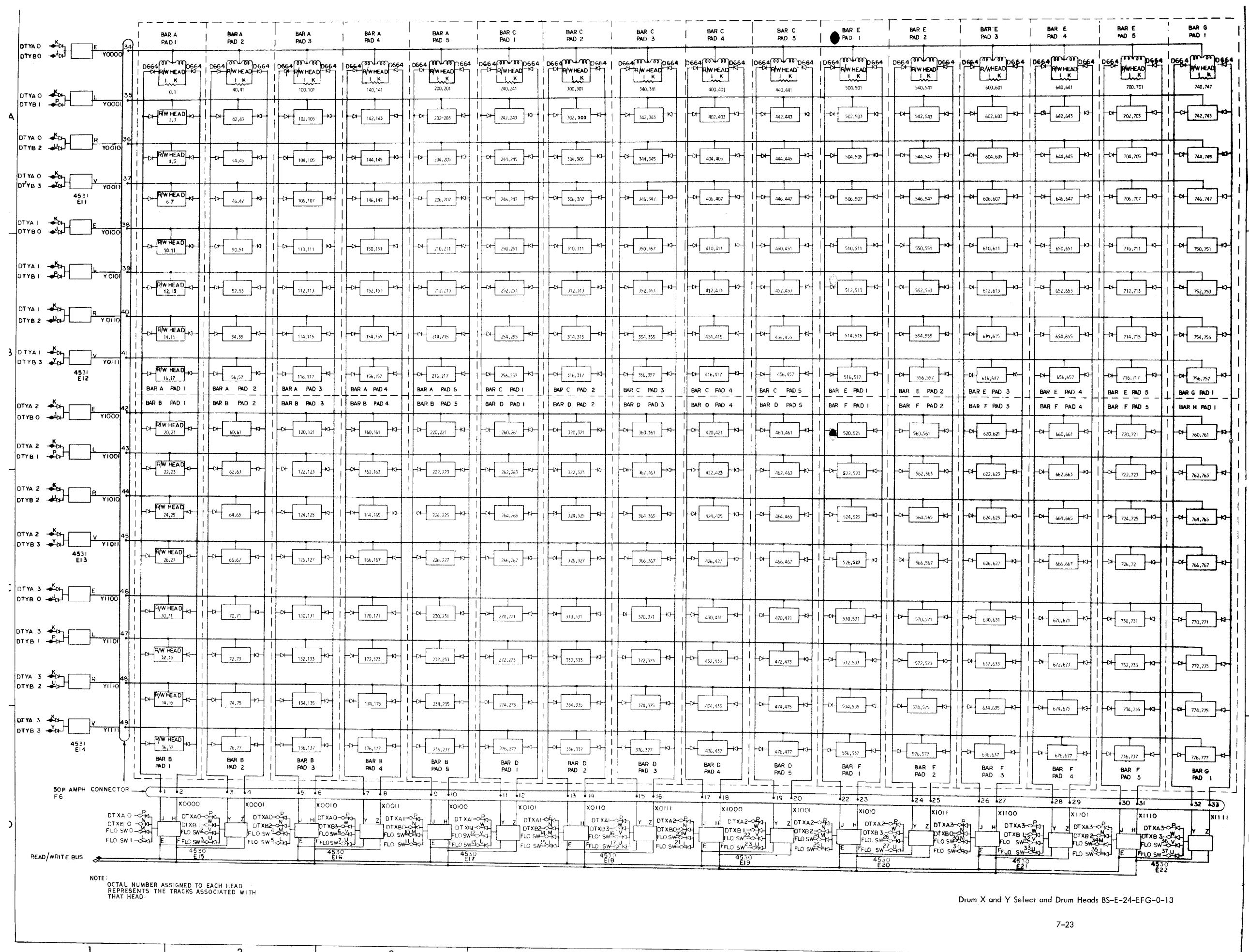
C



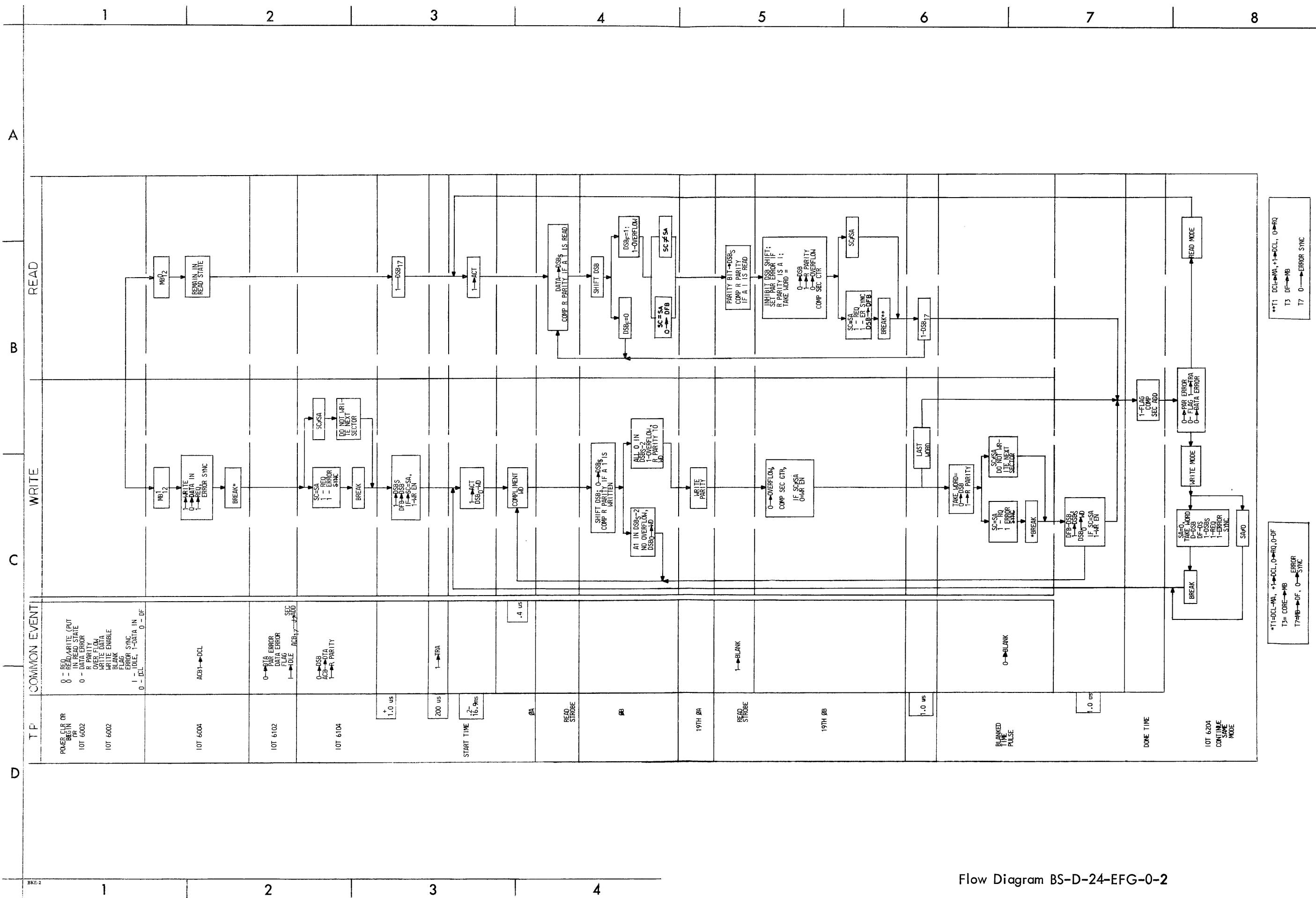
FIELD LOCK OUT SW	OCTAL TRACKS PROTECTED
0	0-17
1	20-37
2	40-57
3	60-77
4	100-117
5	120-137
6	140-157
7	160-177
10	200-217
11	220-237
12	240-257
13	260-277
14	300-317
15	320-337
16	340-357
17	360-377

FIELD LOCK OUT SW	OCTAL TRACKS PROTECTED
20	400-417
21	420-437
22	440-457
23	460-477
24	500-517
25	520-537
26	540-557
27	560-577
30	600-617
31	620-637
32	640-657
33	660-677
34	700-717
35	720-737
36	740-757
37	760-777

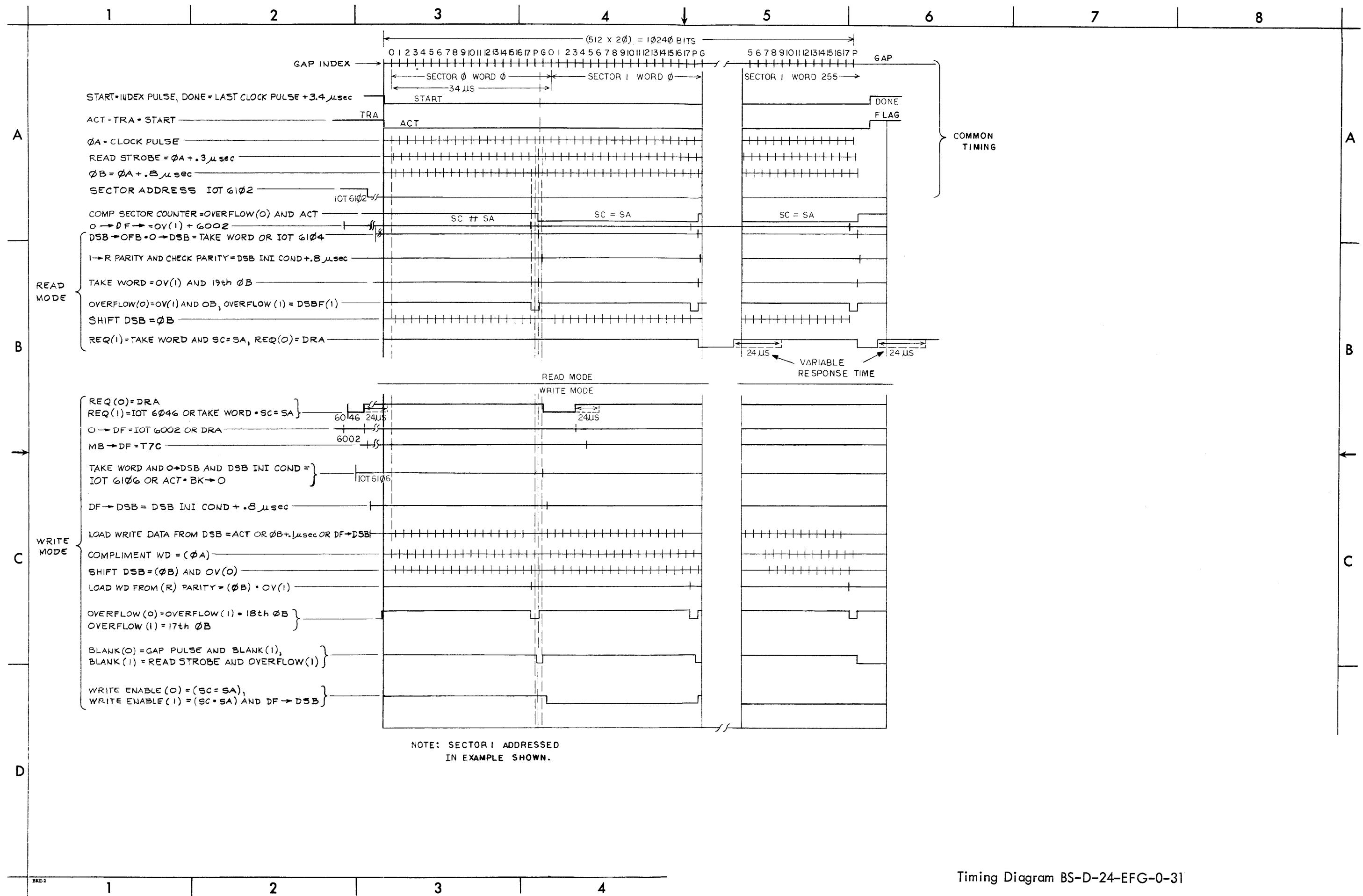
Write Field Lock Out Select BS-D-24-EFG-0-14



Flow Diagram BS-D-24-EFG-0-2



Flow Diagram BS-D-24-EFG-0-2



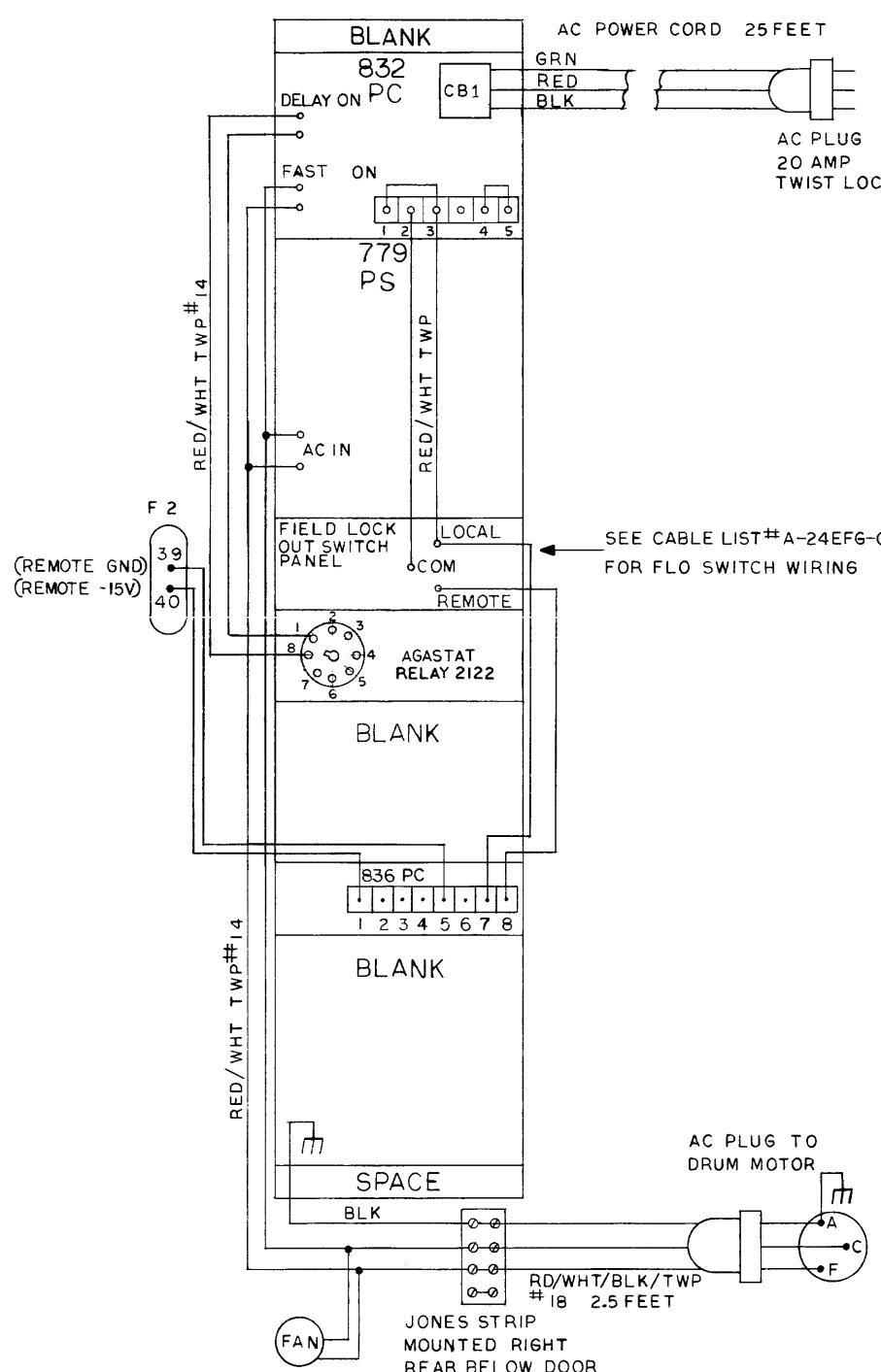
1 | 2 | 3 | 4 | 5 | 6 | 7 | 8

AC WIRING

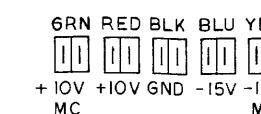
VIEW-FACING REAR DOOR

A

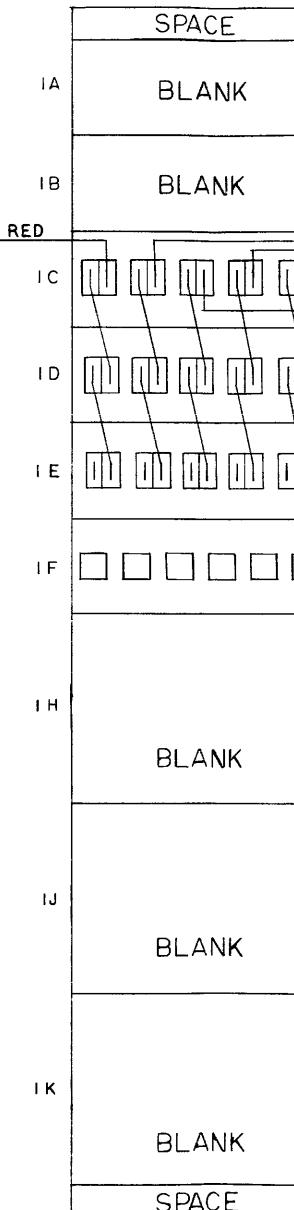
RFAC



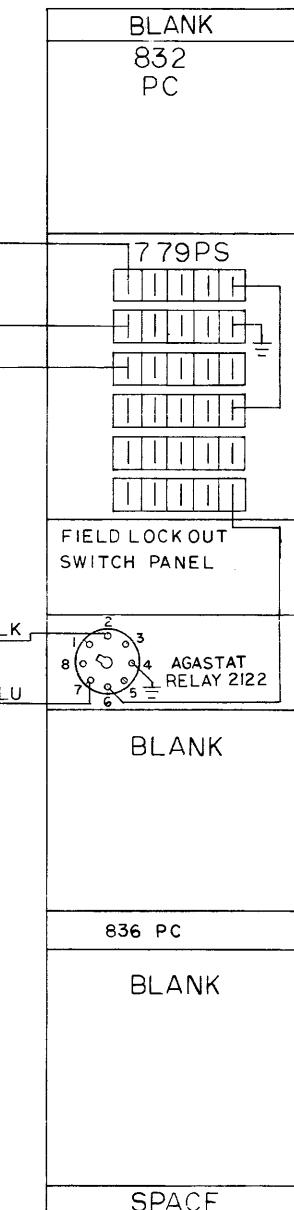
DC WIRING



FROM



REAR

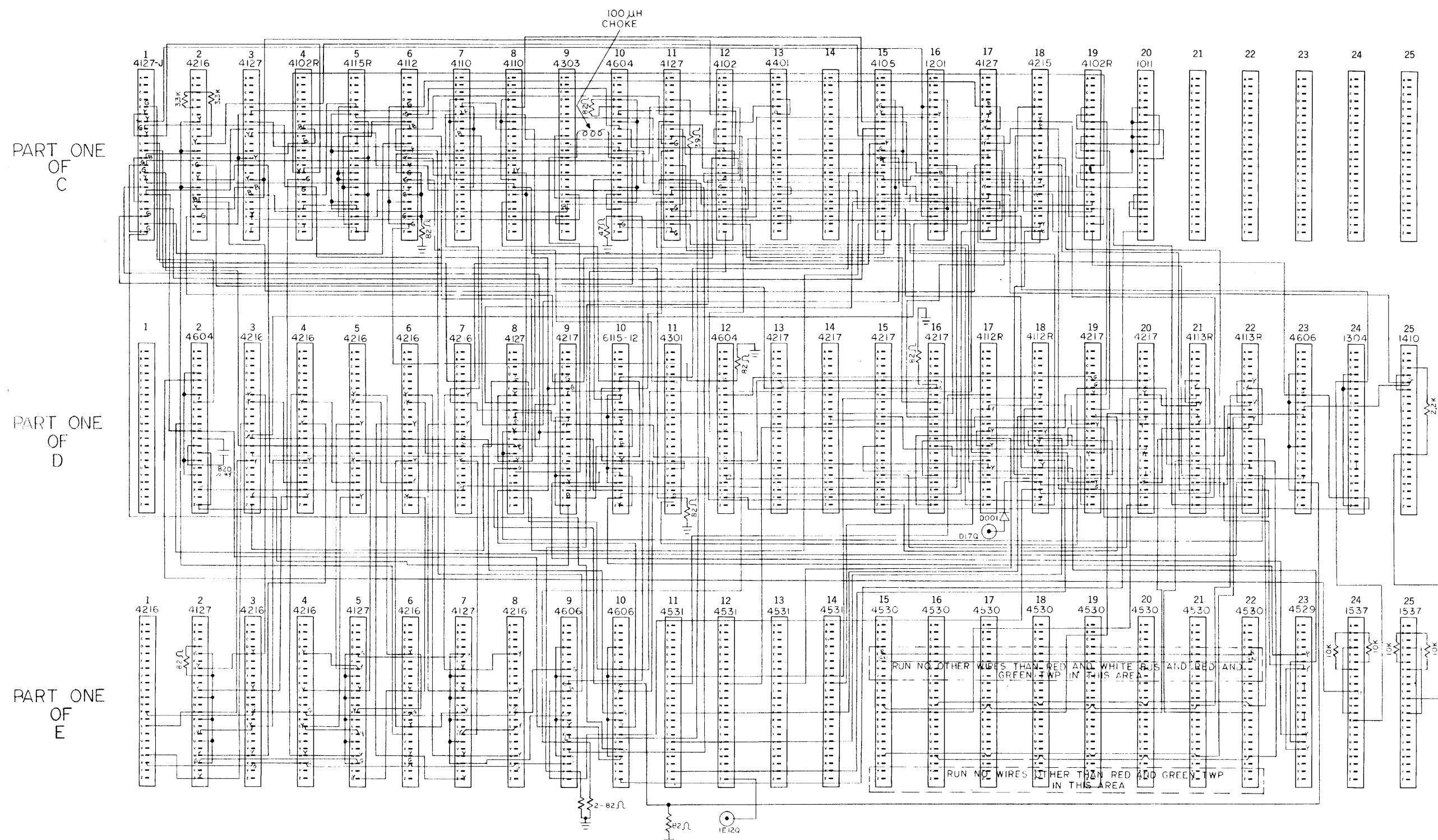


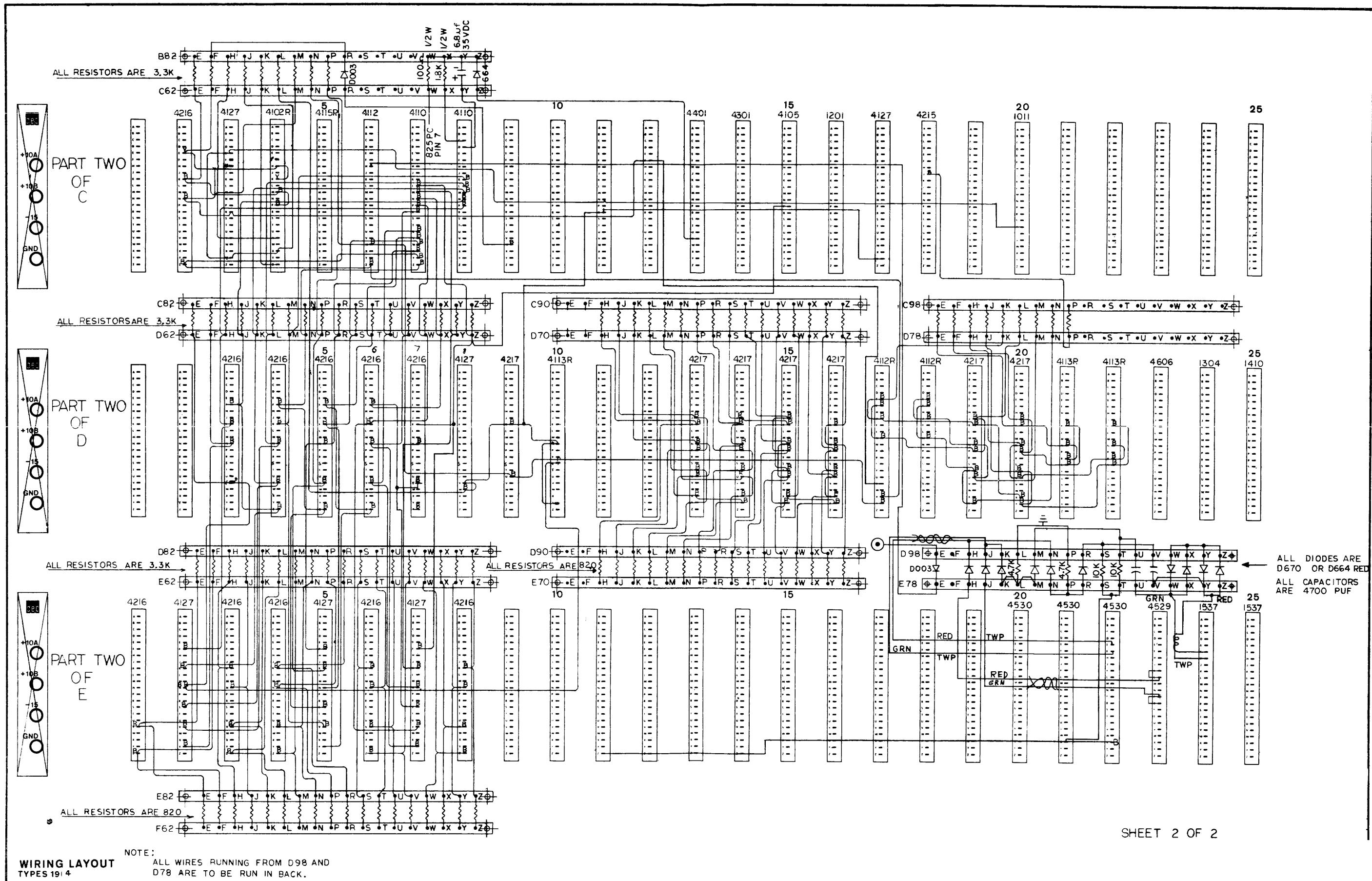
1

1

1

1



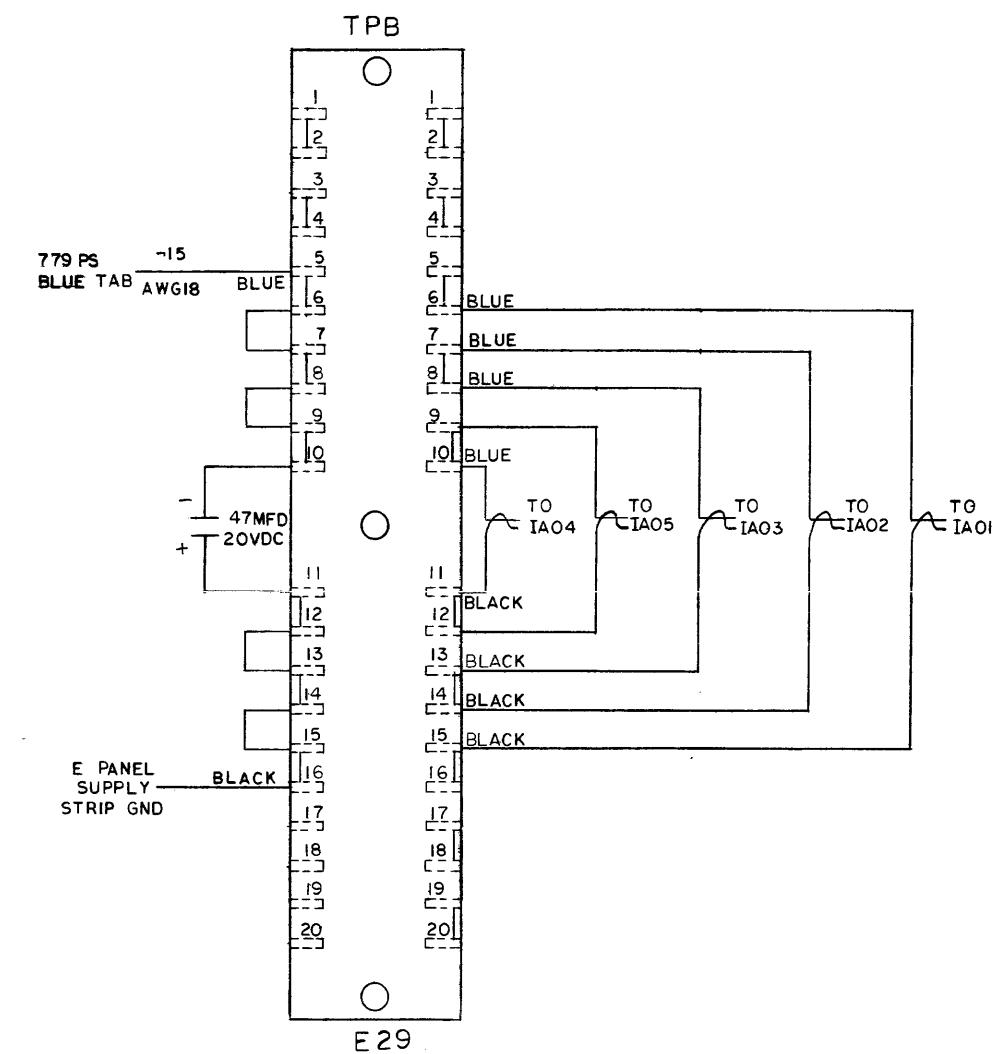
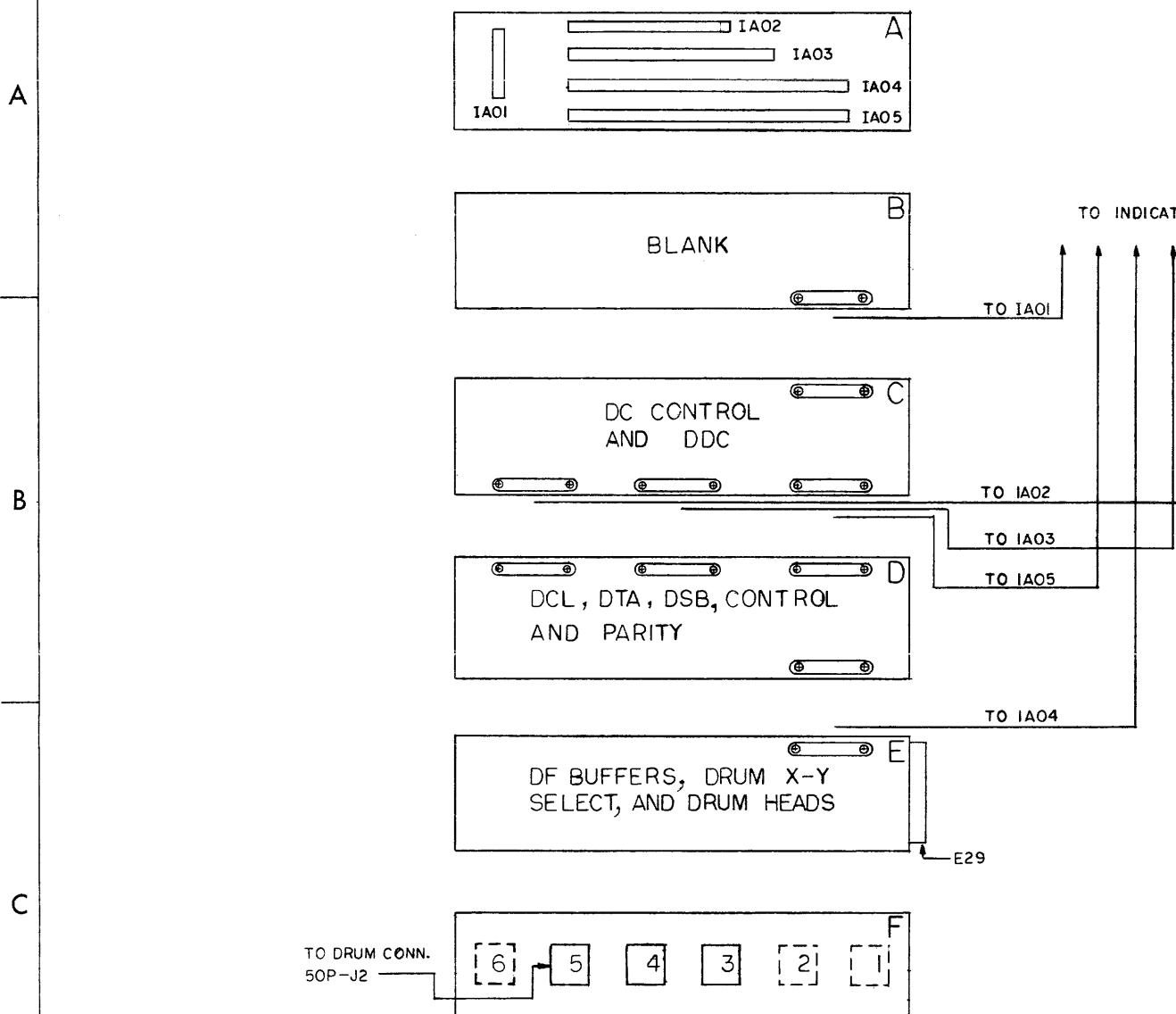


Indicator Cable Breakout and Junction CD-D-24613

1 2 3 4 5 6 7 8

REAR VIEW

INDICATOR CABLE LOCATION



NOTE:

1. = 18 CONNECTION TERMINAL STANDOFF BOARD
2. INDICATORS

NOTE:

AMPH TAPER PIN BLOCK E29 IS DEC STOCK 100A-480065-6

D

BK1-2

1 2 3 4 5 6 7 8

COLOR	NAME	PIN	PIN	REMARKS
RED/WHT	FLO SW 0	1E15M	SW 0/COM	
	SW 1	L	SW 1/COM	
	2	V	SW 2/COM	
	3	U	3	
	4	1E16M	4	
	5	L	5	
	6	V	6	
	7	U	7	
	10	1E17M	10	
	11	L	11	
	12	V	12	
	13	U	13	
	14	1E18M	14	
	15	L	15	
	16	V	16	
	17	U	17	
	20	1E19M	20	
	21	L	21	
	22	V	22	
	23	U	23	
	24	1E20M	24	
	25	L	25	
	26	V	26	
RED/WHT	FLO SW 27	U	SW 27/COM	

Field Lock Out Switch Panel WL-A-24-EFG-0-12 (Sheet 1)

Field Lock Out Switch Panel WL-A-24-EFG-0-12 (Sheet 2)

JACK <input checked="" type="checkbox"/>	PLUG <input type="checkbox"/>	LOCATION, LENGTH, ROUTE			MARK 1A02
FEMALE <input checked="" type="checkbox"/>	MALE <input type="checkbox"/>	50" LONG			
COLOR	PIN	PIN	NAME	REMARKS	
W/ BLK (X)		A			
W/ BRN (Z)		B			
W/ RED (R)		C			
W/ ORN (O)		D			
W/ YEL (Y)		E			
W/ GRN (N)	C98E	F	DTR ₀ ¹		
W/ BLU (B)	C98F	H	DTR ₁ ¹		
W/ VIO (V)	C98H	J	DTR ₂ ¹		
W/ GRY (G)	C98J	K	DTR ₃ ¹		
WHT (W)		L			
W/ BLK (X)	C98K	M	DTR ₄ ¹		
W/ BRN (Z)	C98L	N	DTR ₅ ¹		
W/ RED (R)	C98M	P	DTR ₆ ¹		
W/ ORN (O)	C98N	R	DTR ₇ ¹		
W/ YEL (Y)	C98P	S	STR ¹		
W/ GRN (N)		T			
W/ BLU (B)		U			
W/ VIO (V)	B82F	V	READ		
W/ GRY (G)	B82E	W	WRITE		
WHT (W)		X			
BLUE AND BLK TWP.	E29/7R	Y	-15		
	E29/14R	Z	GND		

Drum Track Address to Indicator Panel CL-A-24-EFG-0-22

JACK <input checked="" type="checkbox"/>	PLUG <input type="checkbox"/>	LOCATION, LENGTH, ROUTE			MARK 1A03
FEMALE <input checked="" type="checkbox"/>	MALE <input type="checkbox"/>	44" LONG			
COLOR	PIN	PIN	NAME	REMARKS	
W/ BLK (X)		A			
W/ BRN (Z)		B			
W/ RED (R)	C90H	C	DCL ₂ ¹		
W/ ORN (O)	C90J	D	DCL 3		
W/ YEL (Y)	C90K	E	DCL 4		
W/ GRN (N)	C90L	F	DCL 5		
W/ BLU (B)	C90M	H	DCL 6		
W/ VIO (V)	C90N	J	DCL 7		
W/ GRY (G)	C90P	K	DCL ₈ ¹		
WHT (W)		L			
W/ BLK (X)	C90R	M	DCL ₉ ¹		
W/ BRN (Z)	C90S	N	DCL 10		
W/ RED (R)	C90T	P	DCL 11		
W/ ORN (O)	C90U	R	DCL 12		
W/ YEL (Y)	C90V	S	DCL 13		
W/ GRN (N)	C90W	T	DCL 14		
W/ BLU (B)	C90X	U	DCL 15		
W/ VIO (V)	C90Y	V	DCL 16		
W/ GRY (G)	C90X	W	DCL ₁₇ ¹		
WHT (W)		X			
BLUE AND	E29/8R	Y	-15V		
BLACK TWP	E29/13R	Z	GND		

JACK <input checked="" type="checkbox"/>	PLUG <input type="checkbox"/>	LOCATION, LENGTH, ROUTE		MARK
FEMALE <input checked="" type="checkbox"/>	MALE <input type="checkbox"/>	38" LONG		1A05
COLOR	PIN	PIN	NAME	REMARKS
W/ BLK (X)	C82E	A	DSB ₀ ¹	
W/ BRN (Z)	C82F	B	DSB 1	
W/ RED (R)	C82H	C	DSB 2	
W/ ORN (O)	C82J	D	DSB 3	
W/ YEL (Y)	C82K	E	DSB 4	
W/ GRN (N)	C82L	F	DSB 5	
W/ BLU (B)	C82M	H	DSB 6	
W/ VIO (V)	C82N	J	DSB 7	
W/ GRY (G)	C82P	K	DSB ₈ ¹	
WHT (W)		L		
W/ BLK (X)	C82R	M	DSB ₉ ¹	
W/ BRN (Z)	C82S	N	DSB 10	
W/ RED (R)	C82T	P	DSB 11	
W/ ORN (O)	C82U	R	DSB 12	
W/ YEL (Y)	C82V	S	DSB 13	
W/ GRN (N)	C82W	T	DSB 14	
W/ BLU (B)	C82X	U	DSB 15	
W/ VIO (V)	C82Y	V	DSB 16	
W/ GRY (G)	C82Z	W	DSB ₁₇ ¹	
WHT (W)		X		
BLUE AND BLACK	E29/9R	Y	-15V	
TWP	E29/12R	Z	GND	

JACK <input checked="" type="checkbox"/>	PLUG <input type="checkbox"/>	LOCATION, LENGTH, ROUTE			MARK
FEMALE <input checked="" type="checkbox"/>	MALE <input type="checkbox"/>	44" LONG			1A04
COLOR	PIN	PIN	NAME		REMARKS
W/ BLK (X)	D82E	A	DFB ¹ ₀		
W/ BRN (Z)	D82F	B	DFB 1		
W/ RED (R)	D82H	C	DFB 2		
W/ ORN (O)	D82J	D	DFB 3		
W/ YEL (Y)	D82K	E	DFB 4		
W/ GRN (N)	D82L	F	DFB 5		
W/ BLU (B)	D82M	H	DFB 6		
W/ VIO (V)	D82N	J	DFB 7		
W/ GRY (G)	D82P	K	DFB ¹ ₈		
WHT (W)		L			
W/ BLK (X)	D82R	M	DFB ¹ ₉		
W/ BRN (Z)	D82S	N	DFB ¹ ₁₀		
W/ RED (R)	D82T	P	DFB ¹ ₁₁		
W/ ORN (O)	D82U	R	DFB 12		
W/ YEL (Y)	D82V	S	DFB 13		
W/ GRN (N)	D82W	T	DFB 14		
W/ BLU (B)	D82X	U	DFB 15		
W/ VIO (V)	D82Y	V	DFB 16		
W/ GRY (G)	D82Z	W	DFB ¹ ₁₇		
WHT (W)		X			
BLUE AND	E29/10R	Y	-15		
BLACK TWP	E29/11R	Z	GND		

JACK <input checked="" type="checkbox"/>	PLUG <input type="checkbox"/>	LOCATION, LENGTH, ROUTE					
FEMALE <input checked="" type="checkbox"/>	MALE <input type="checkbox"/>	F3					
COLOR	PIN	PIN	NAME	COLOR	PIN	PIN	NAME*
WHITE	C22F	1	DF ⁰ → MB ⁰	WHITE	E04T	26	MBD7 → DF7
	J	2	1		M	27	8
	L	3	2		H	28	9
	N	4	3		E06H	29	10
	R	5	4		M	30	11
	T	6	5		T	31	12
	V	7	6		Y	32	13
	X	8	7		E08Y	33	14
	C22Z	9	8		T	34	15
	C23F	10	9		M	35	16
	J	11	10		H	36	MBD17 → DF17
	L	12	11		C24T	37	DCL5 → MA5
	N	13	12		V	38	6
	R	14	13		X	39	7
	T	15	14		C24Z	40	8
	V	16	15		C25F	41	9
	X	17	16		J	42	10
	C23Z	18	DF17 → MB17		L	43	11
	E01T	19	MBD0 → DF0		N	44	12
	Y	20	1		R	45	13
	E03H	21	2		T	46	14
	M	22	3		V	47	15
	T	23	4		X	48	16
	Y	24	5	WHITE	C25Z	49	17
WHITE	E04Y	25	MBD ⁰ → DF ⁰	BLACK	GND, LUG	50	GND.

JACK <input checked="" type="checkbox"/>	PLUG <input type="checkbox"/>	LOCATION, LENGTH, ROUTE		*ONLY USED IF SPECIFIED			
FEMALE <input checked="" type="checkbox"/>	MALE <input type="checkbox"/>	F4					
COLOR	PIN	PIN	NAME	COLOR	PIN	PIN	NAME
		1				26	
		2				27	
WHITE	D13L	3	ACB2 → DCL2			28	
	↑	R	4	3		29	
		V	5	4		30	
	↓	Z	6	5		31	
	D14Z	7	6			32	
		V	8	7		33	
		R	9	8		34	
	↓	L	10	9	WHT	TA/PIN 1	35 TEM SW (TA)*
	D15L	11	10	BLK	TWP	TA/PIN 2	36 TA GND*
		R	12	11			37
		V	13	12	RED	E PANEL +10 MC	38 +10 MC
	↓	Z	14	13	WHT	836PC-5	39 ND REMOTE TURN ON
	D16Z	15	14	BRN	TWP	836PC-1	40 -15 REMOTE TURN ON
		V	16	15			41
		R	17	16	GRY/BLK/TWP	E09Y	42 DATA REQ ANS
	↓	L	18	ACB17 → DCL17	↑	C10E	43 BEGIN
	C04Z	19	DRUM FLAG			C11X	44 T7B
	D17Z	20	PE ⁰ • DE ⁰			E09U	45 IOT 6002
	C12X	21	DATA REQ.			D13F	46 IOT 6004
	C04N	22	DATA IN			D12E	47 IOT 6102
	C24L	23	DCL 2			D11Y	48 IOT 6104
	↓	C24N	24	DCL 3	GRY/BLK/TWP	C06X	49 IOT 6204
WHITE	C24R	25	DCL4 → MA4	BLK		GND LUG	50 GND

JACK	<input checked="" type="checkbox"/>	PLUG	<input type="checkbox"/>	LOCATION, LENGTH, ROUTE				
FEMALE	<input checked="" type="checkbox"/>	MALE	<input type="checkbox"/>	F5				
COLOR	PIN	PIN	NAME	COLOR	PIN	PIN	NAME	
RED	E15 J	1	X0	RED	E21 J	26	X14	
GREEN	H	2	X0	GREEN	H	27	X14	
RED	Y	3	X1	RED	Y	28	X15	
GREEN	E15 Z	4	X1	GREEN	E21 Z	29	X15	
RED	E16 J	5	X2	RED	E22 J	30	X16	
GREEN	H	6	X2	GREEN	H	31	X16	
RED	Y	7	X3	RED	Y	32	X17	
GREEN	E16 Z	8	X3	GREEN	E22 Z	33	X17	
RED	E17 J	9	X4	BLACK	E11 E	34	Y0	
GREEN	H	10	X4		L	35	Y1	
RED	Y	11	X5		R	36	Y2	
GREEN	E17 Z	12	X5		E11 V	37	Y3	
RED	E18 J	13	X6		E12 E	38	Y4	
GREEN	H	14	X6		L	39	Y5	
RED	Y	15	X7		R	40	Y6	
GREEN	E18 Z	16	X7		E12 V	41	Y7	
RED	E19 J	17	X10		E13 E	42	Y10	
GREEN	H	18	X10		L	43	Y11	
RED	Y	19	X11		R	44	Y12	
GREEN	E19 Z	20	X11		E13 V	45	Y13	
	SPARE	21			E14 E	46	Y14	
RED	E20 J	22	X12		L	47	Y15	
GREEN	H	23	X12		R	48	Y16	
RED	Y	24	X13		E14 V	49	Y17	
GREEN	E20 Z	25	X13	BLACK	GND LUG	50	GND	

TAPER PIN CONNECTION

JACK <input type="checkbox"/>	PLUG <input checked="" type="checkbox"/>	LOCATION, LENGTH, ROUTE - AT PLUG END. USE TRIPLE CONDUCTOR SHIELDED. JUMPER IN SPARES AS NEEDED. PLUG END MUST NOT BE CONNECTED WHILE SOLDERING LOGIC END.					
FEMALE <input type="checkbox"/>	MALE <input checked="" type="checkbox"/>						
COLOR	PIN	PIN	NAME	COLOR	PIN	PIN	NAME
RED	E25H	1	START	RED	E25H	26	START
BLACK	E	2	CT CLOCK	BLACK	E	27	CT CLOCK
GREEN	F	3	FIN. #1	GREEN	F	28	FIN. #7
SHIELD	GND	4	GND	SHIELD	GND	29	GND
RED	H	5	START	RED	H	30	START
BLACK	E	6	CT CLOCK	BLACK	E	31	CT CLOCK
GREEN	F	7	FIN. #2	GREEN	F	32	FIN. #8
SHIELD	GND	8	GND	SHIELD	E25GND	33	GND
RED	H	9	START			34	
BLACK	E	10	CT CLOCK			35	
GREEN	F	11	FIN. #3			36	
SHIELD	GND	12	GND			37	
RED	H	13	START			38	
BLACK	E	14	CT CLOCK			39	
GREEN	F	15	FIN. #4			40	
SHIELD	E25GND	16	GND			41	
		17				42	
RED	E25H	18	START			43	
BLACK	E	19	CT CLOCK	NOTE: SAMPLE ALL CLOCK			44
GREEN	F	20	FIN. #5	HEADS AND INITIALLY			45
SHIELD	GND	21	GND	USE HEAD WITH HIGHEST			46
RED	H	22	START	OUTPUT			47
BLACK	E	23	CT CLOCK			48	
GREEN	F	24	FIN. #6			49	
SHIELD	E25GND	25	GND			50	

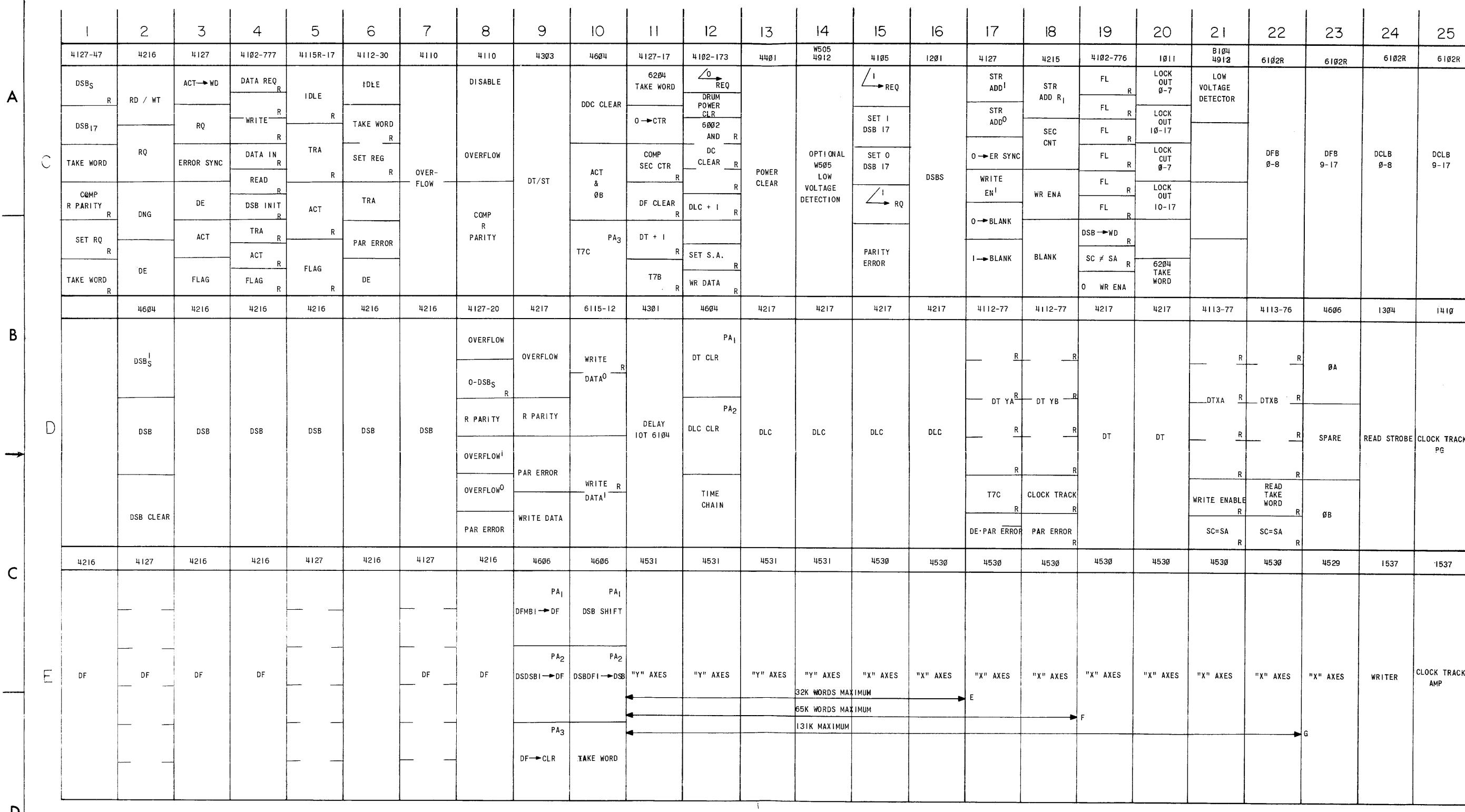
COLOR	NAME	PIN	PIN	REMARKS
GRAY	IOT 6101	2F20E	2H07E/F1	SKIP ON DRUM FLG
GRAY	IOT 6201	2F21E	2H07H/F1	SKIP ON PE ^o DE ^o
WHITE	DRUM FLAG '	2H05P/F2	2H07F/F1	
	DRUM FLAG '	2H07F/F2	2H25L/F2	
BLUE	MB ⁰	1E25A/F3	2E24E	
	1	B	H	
	2	C	K	
	3	D	M	
	4	E	P	
	5	F	S	
	6	G	U	
	7	H	W	
	8	J	2E24Y	
	9	K	2E25E	
	10	L	H	
	11	M	K	
	12	N	M	
	13	P	P	
	14	R	S	
	15	S	U	
	16	T	W	
BLUE	MB17	1E25U/F3	2E25Y	

IOT and IO Skip, Computer Side WL-A-24-EFG-0-27

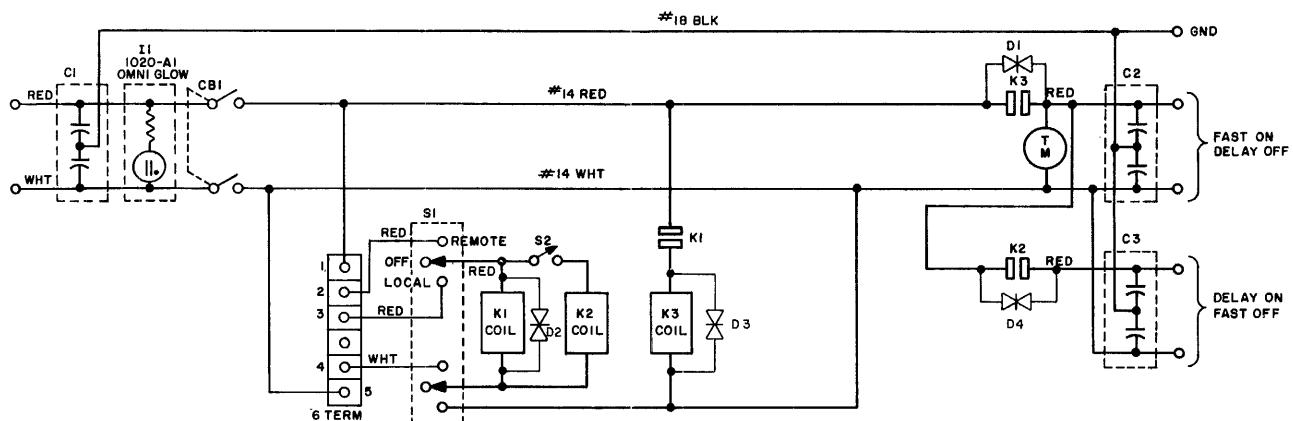
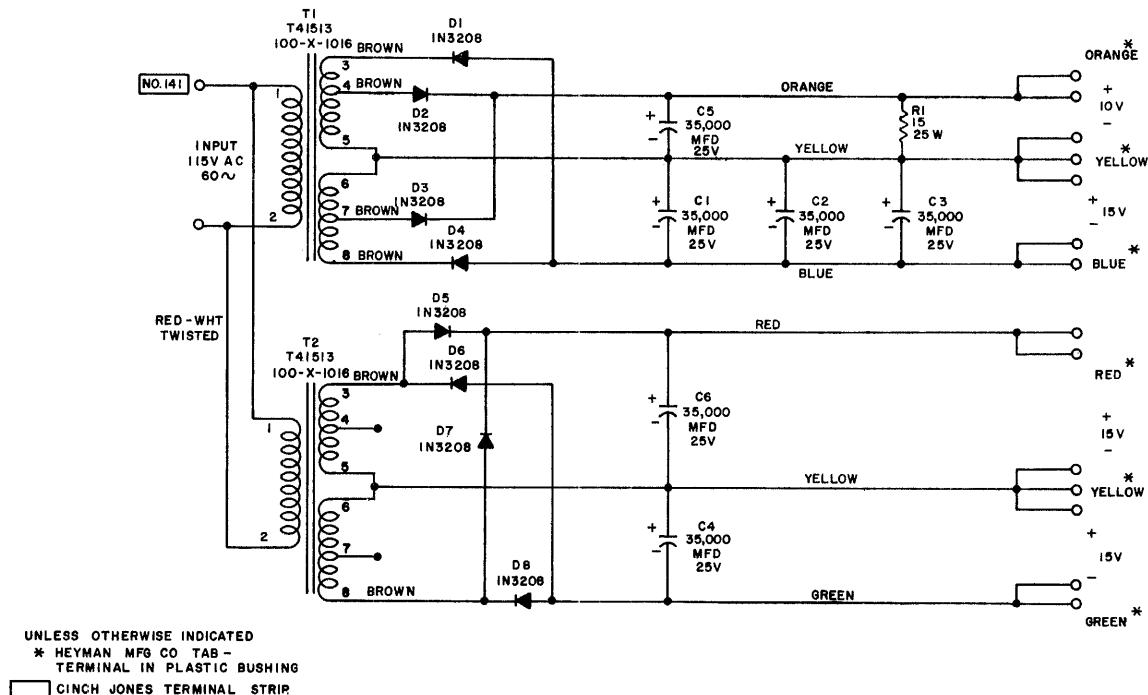
JACK <input type="checkbox"/>	PLUG <input checked="" type="checkbox"/>	LOCATION, LENGTH, ROUTE					
FEMALE <input type="checkbox"/>	MALE <input checked="" type="checkbox"/>	F5-J2 CABLE				10" INSIDE DIMENSION	
COLOR	PIN MALE	PIN MALE	NAME	COLOR	PIN	PIN	NAME
RED 	1	1	X0	RED 	26	26	X14
GRN 	2	2	X0	GRN 	27	27	X14
RED 	3	3	X1	RED 	28	28	X15
GRN 	4	4	X1	GRN 	29	29	X15
RED 	5	5	X2	RED 	30	30	X16
GRN 	6	6	X2	GRN 	31	31	X16
RED 	7	7	X3	RED 	32	32	X17
GRN 	8	8	X3	GRN 	33	33	X17
RED 	9	9	X4	BLK	34	34	Y0
GRN 	10	10	X4		35	35	Y1
RED 	11	11	X5		36	36	Y2
GRN 	12	12	X5		37	37	Y3
RED 	13	13	X6		38	38	Y4
GRN 	14	14	X6		39	39	Y5
RED 	15	15	X7		40	40	Y6
GRN 	16	16	X7		41	41	Y7
RED 	17	17	X10		42	42	Y10
GRN 	18	18	Y10		43	43	Y11
RED 	19	19	X11		44	44	Y12
GRN 	20	20	X11		45	45	Y13
WHT	21	21	SPARE		46	46	Y14
RED 	22	22	X12		47	47	Y15
GRN 	23	23	X12		48	48	Y16
RED 	24	24	X13		49	49	Y17
GRN 	25	25	X13	BLK	50	50	GND

Selection Cable CL-A-24-EFG-0-28

1 2 3 4 5 6 7 8



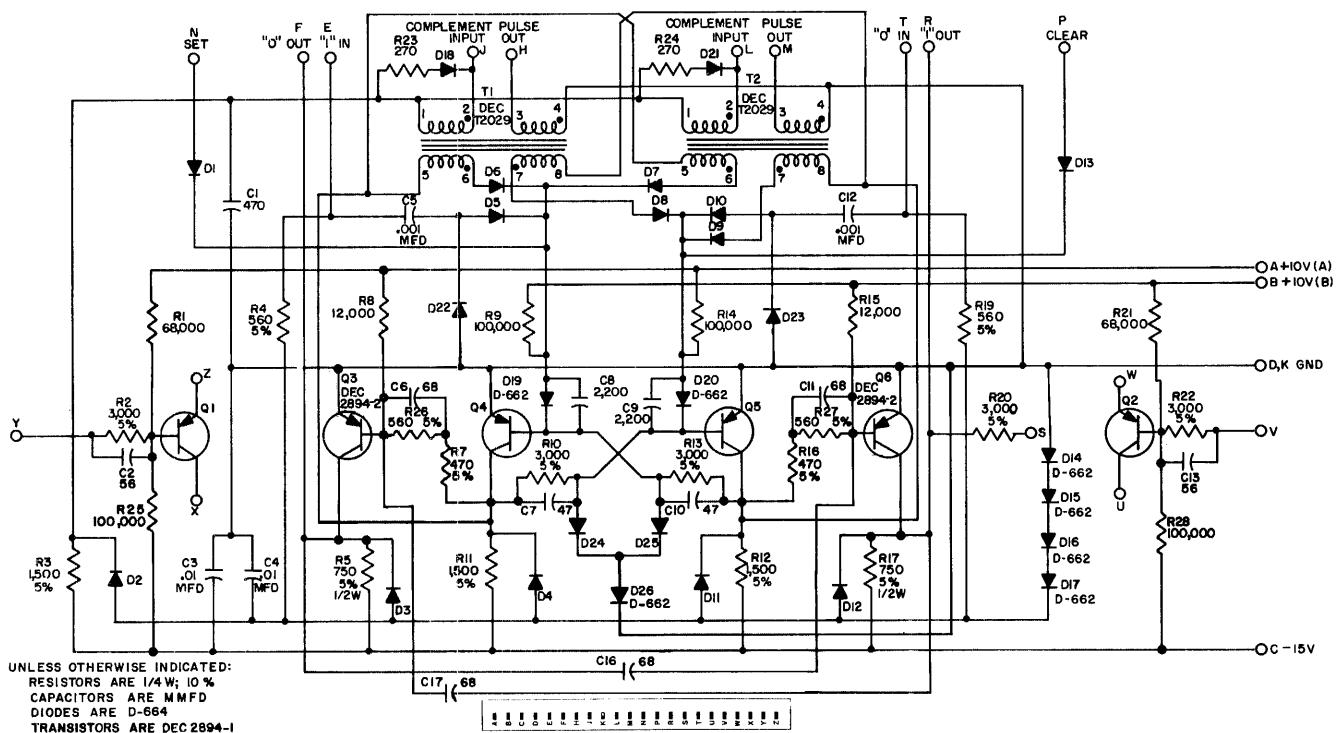
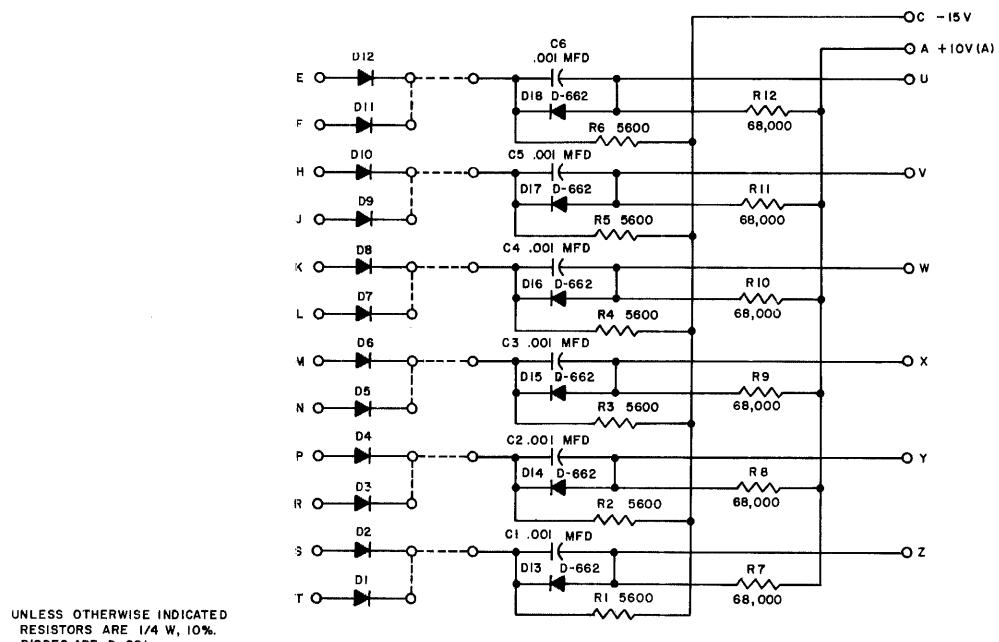
1 2 3 4



NOTES:
 D1, D2, D3, D4, THYRECTOR GENERAL ELECTRIC 20 SP 4B4, 115V
 C1 CAPACITOR 2 X 1 MFD 1000VDC *YAT 1000I
 CORNELL DUBLIER.
 C2 & C3 CAPACITOR BATHTUB-DEC PURCH. SPEC *CAF-0001
 2X .1MFD 600VDC CORNELL DUBLIER.
 S1 TOGGLE SWITCH 3 POS #152P
 S2 TOGGLE SWITCH 3 POS #7805-K3
 K1 RELAY #1040-8-687 NORMALLY OPEN 115VAC COIL 3-5 SEC DELAY
 QUICK OPERATE, SLOW RELEASE.
 K2 RELAY #1040-8-58 NORMALLY OPEN 115 VAC COIL 3-5 SEC DELAY
 SLOW OPERATE QUICK RELEASE.
 K3 RELAY #EM-1 115VAC EBERT ELECTRONICS.
 CBI CIRCUIT BREAKER #190-220-101 20AMPS 250V, 60 CYC-CURVE 4

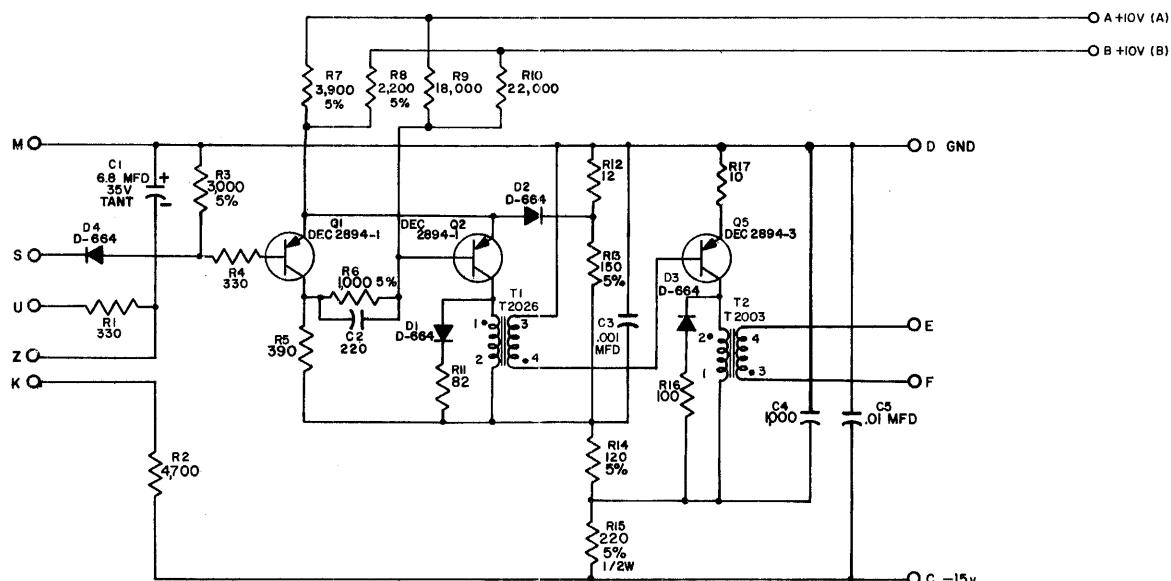
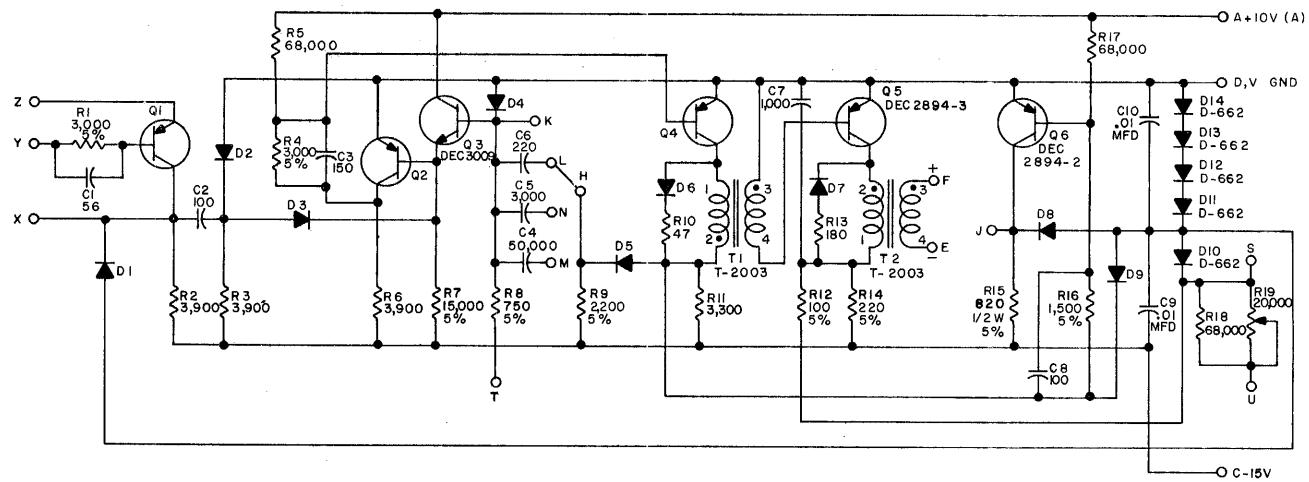
Power Supply RS-779

Power Control Panel RS-832



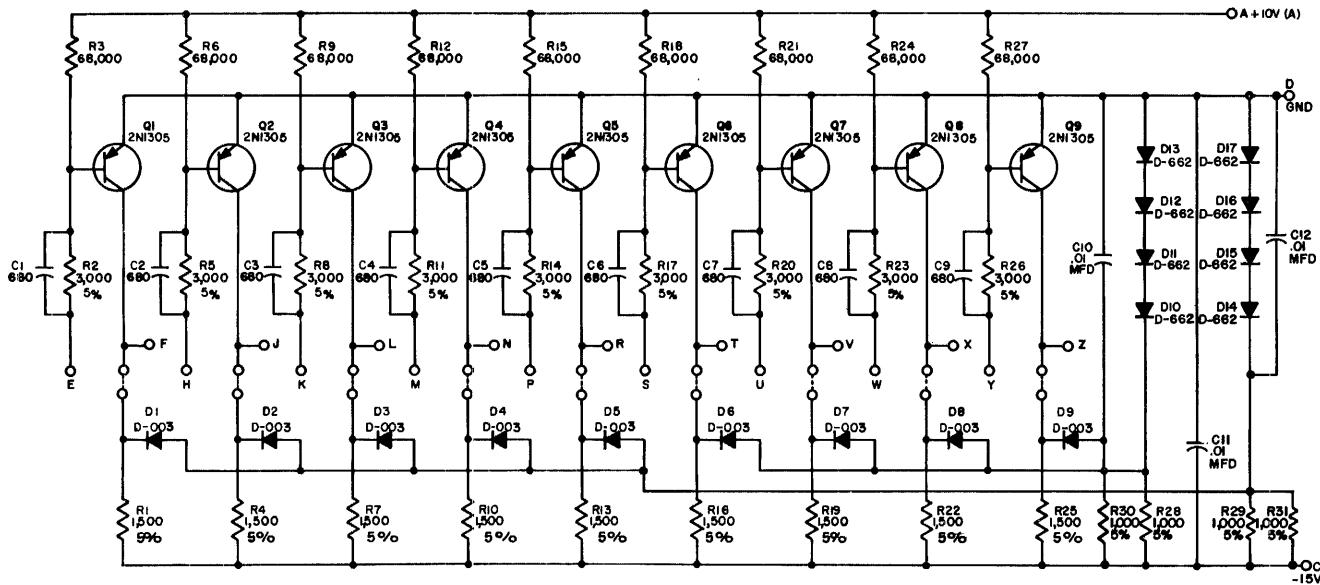
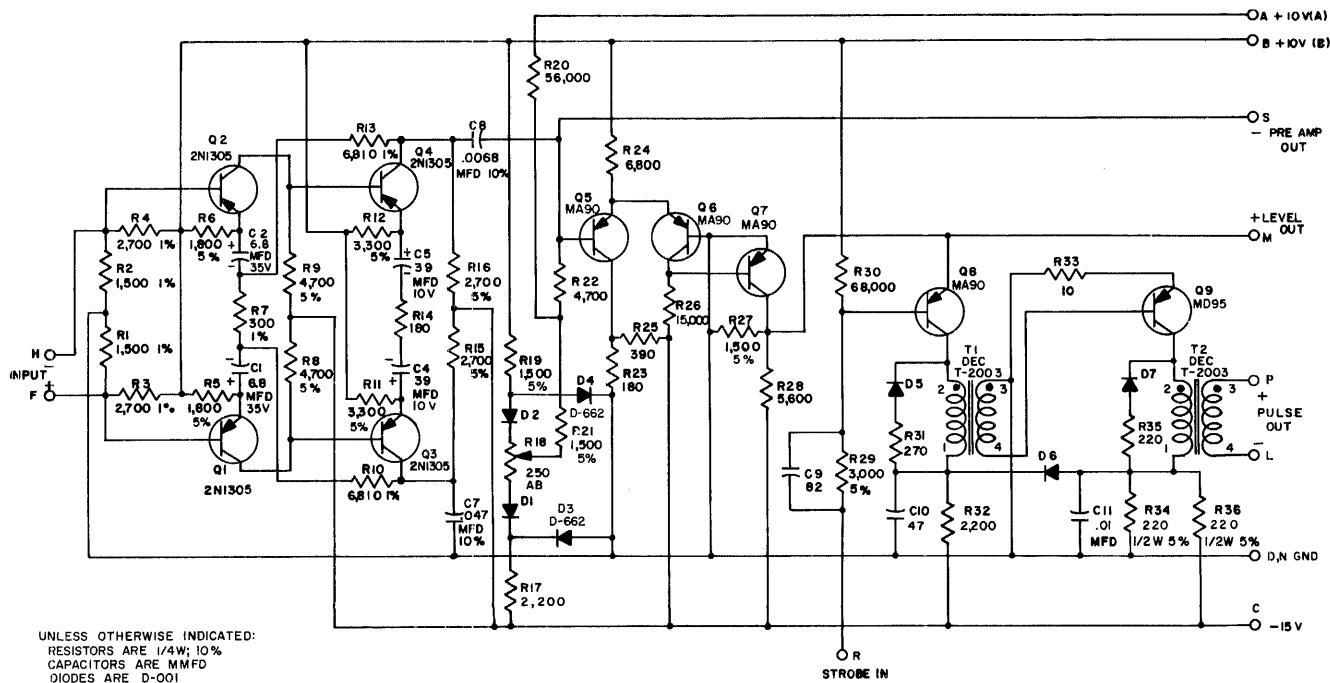
Diode RS-1011

Flip-Flop RS-1201



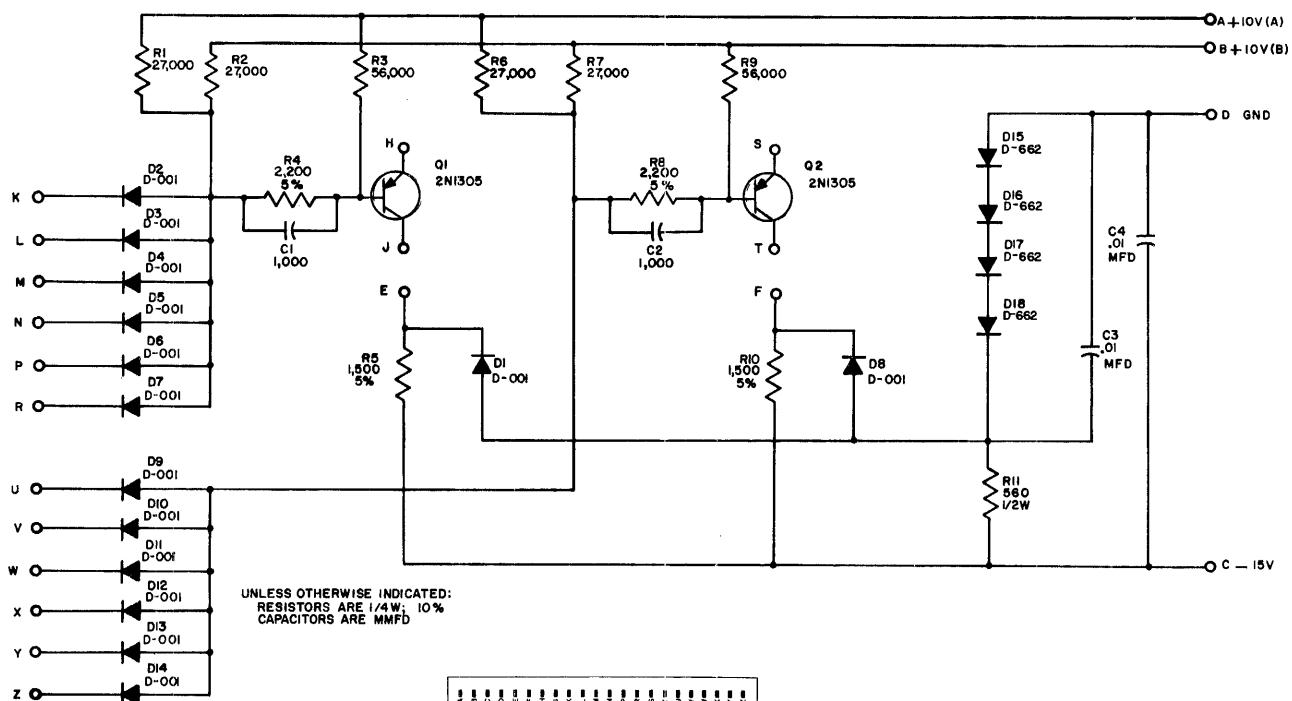
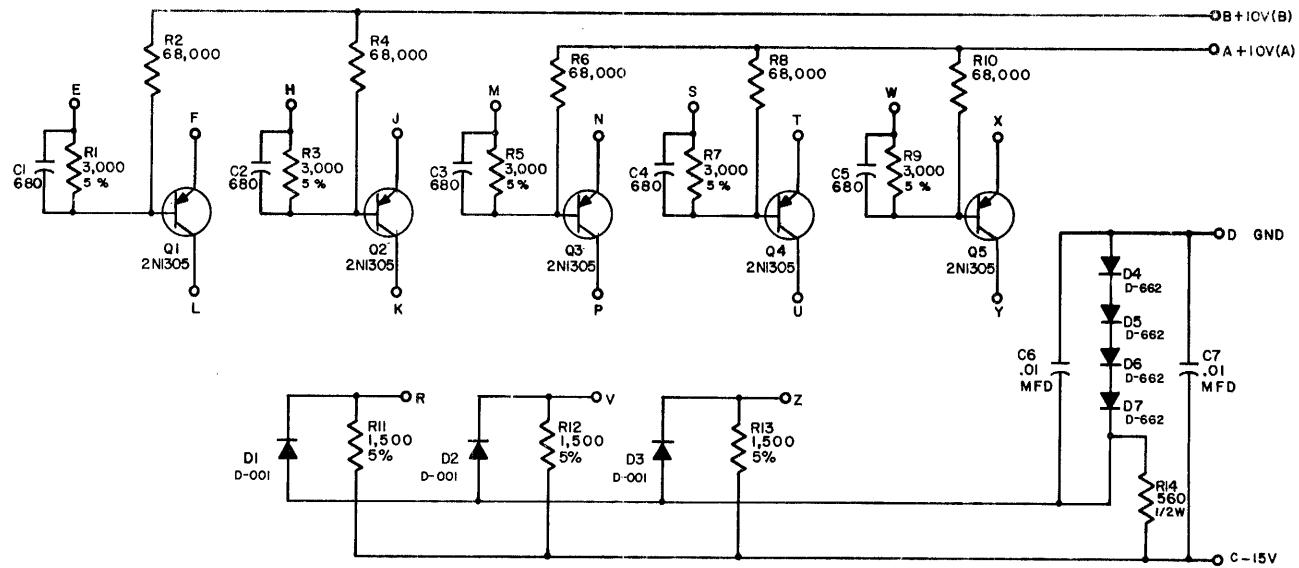
Delay RS-1304

Pulse Generator RS-1410



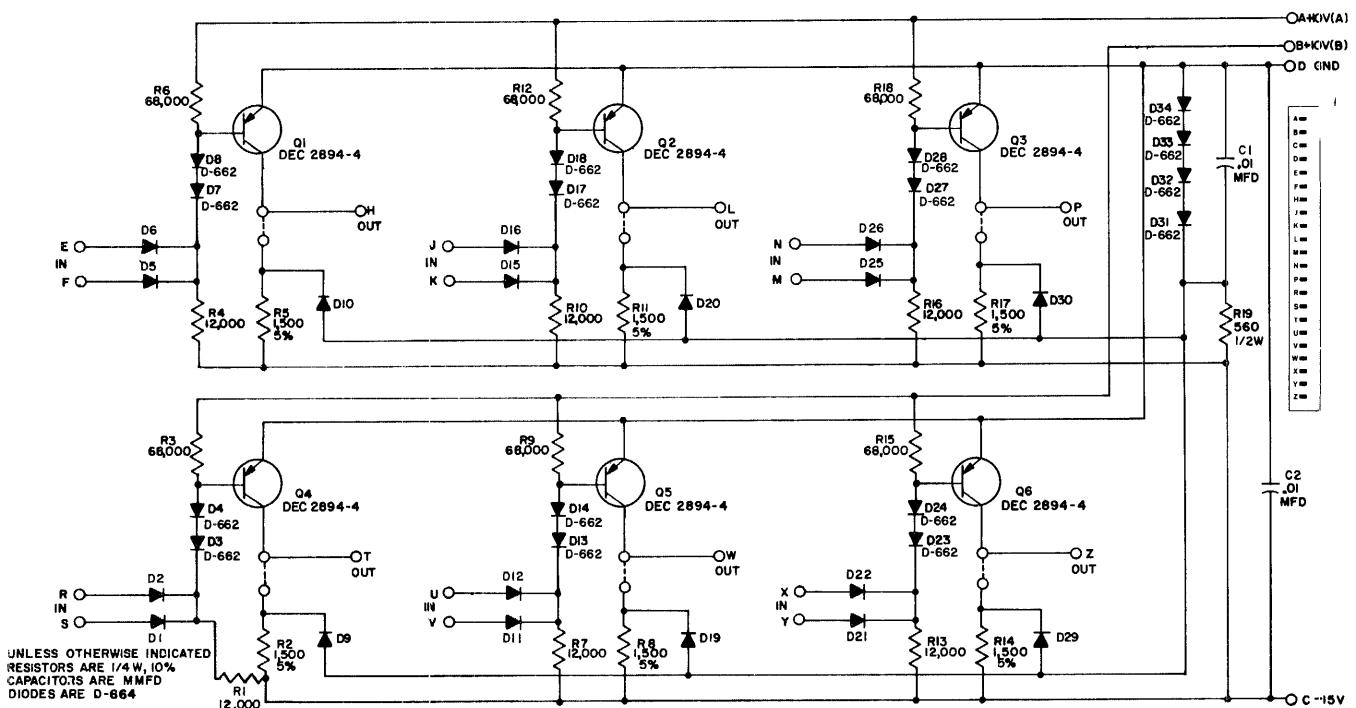
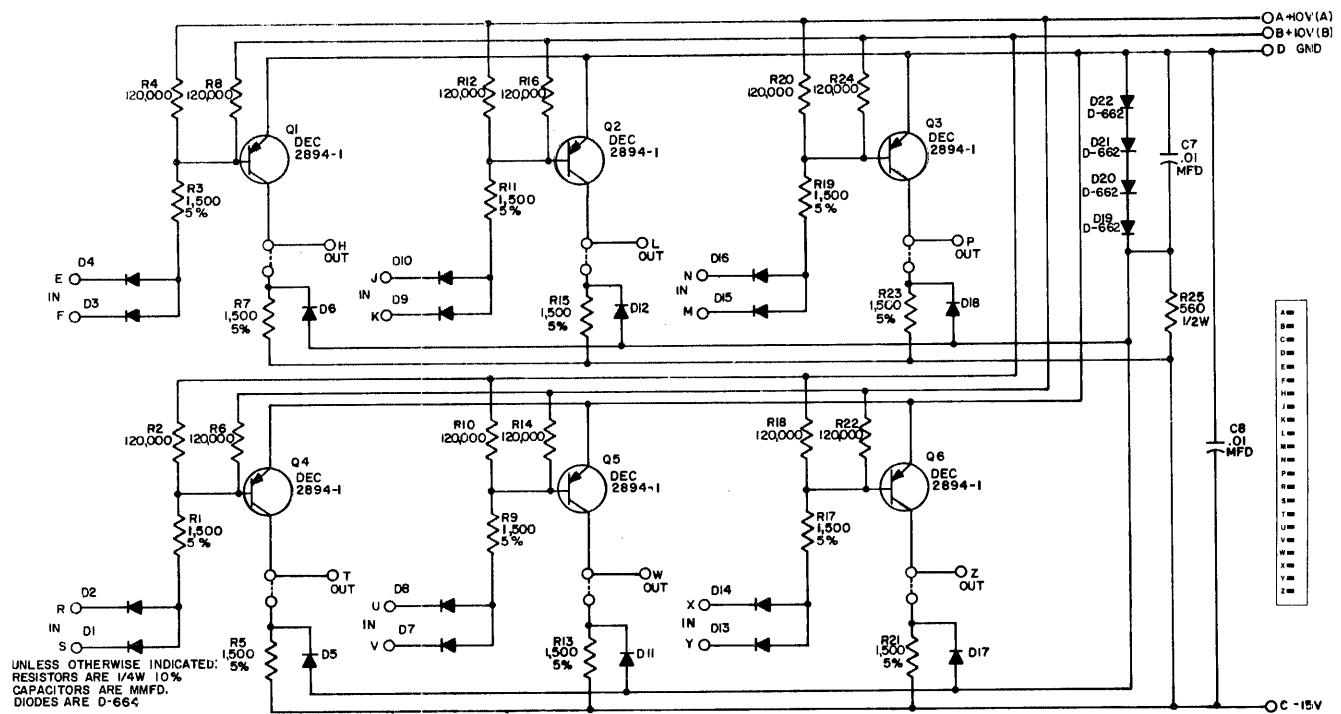
Drum Sense Amplifier RS-1537

Inverter RS-4102



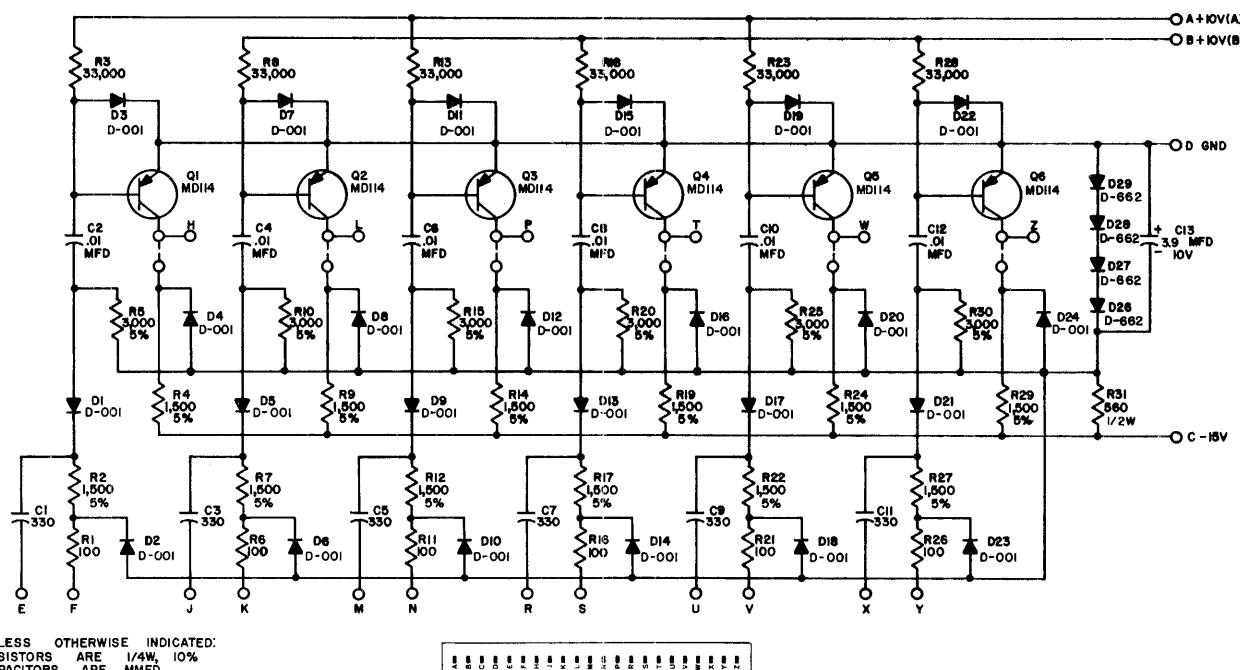
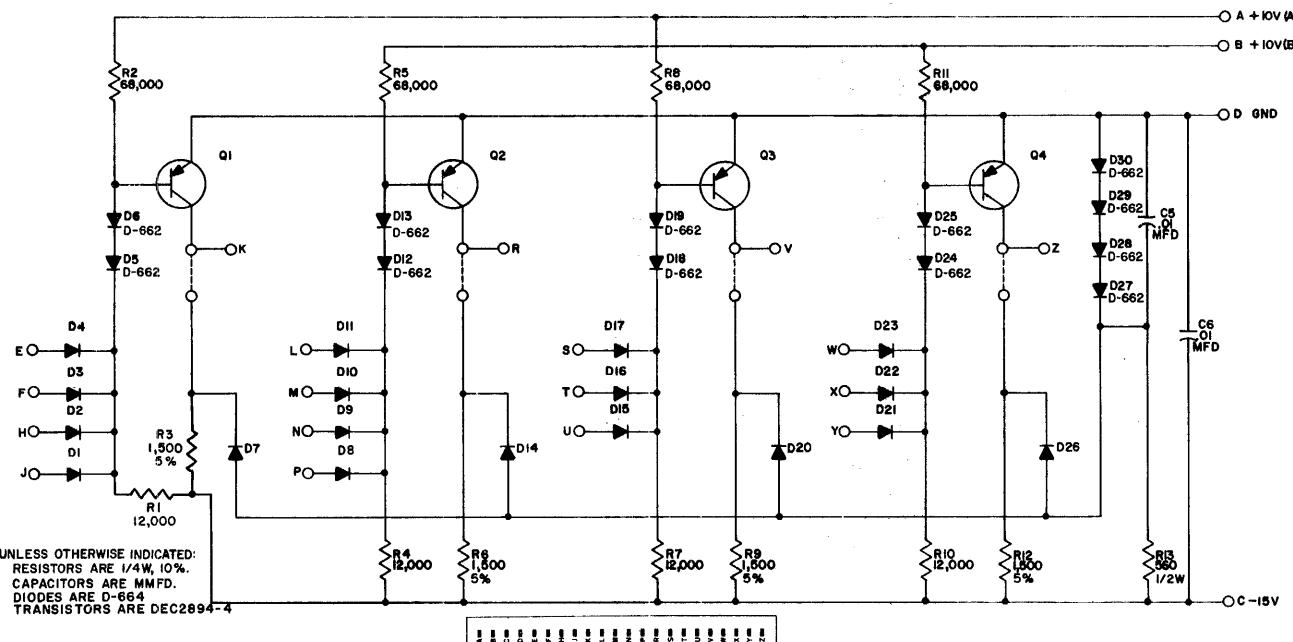
Inverter RS-4105

Diode Unit RS-4110



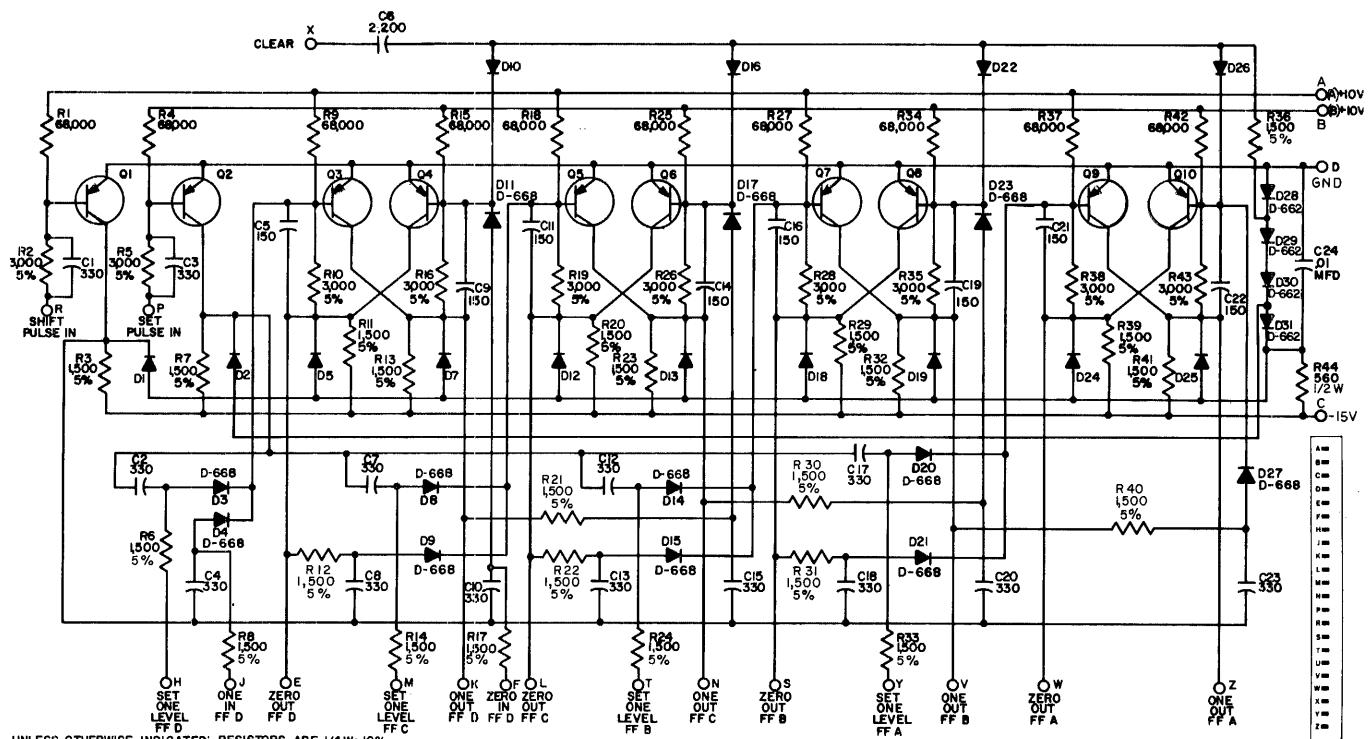
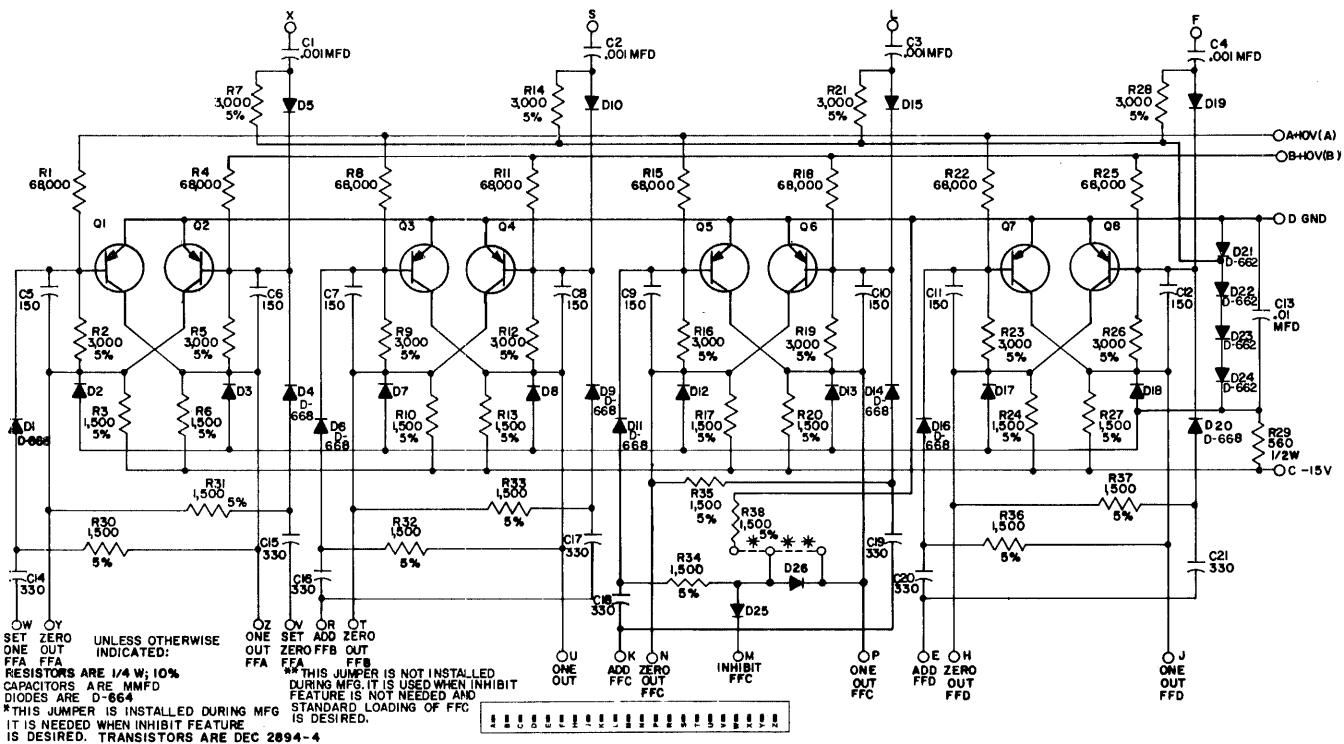
Diode RS-4112

Diode RS-4113



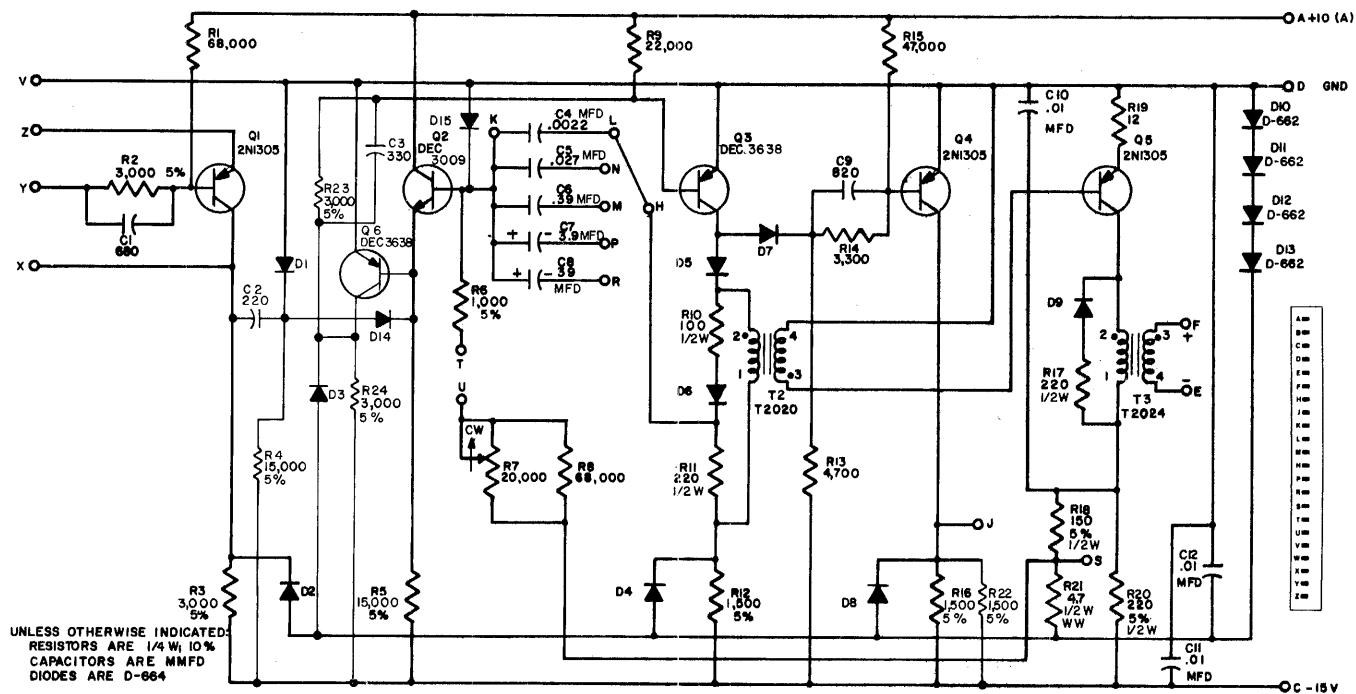
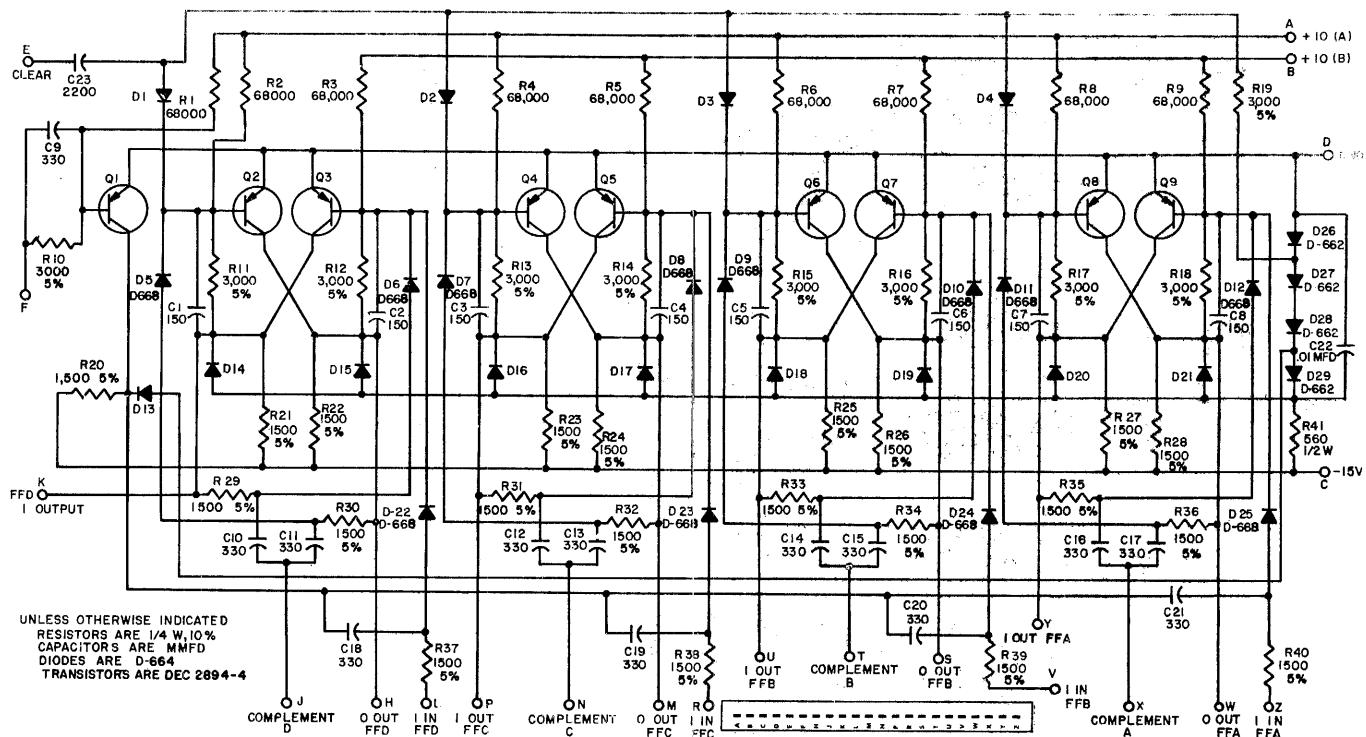
Diode RS-4115

Capacitor-Diode-Inverter RS-4127



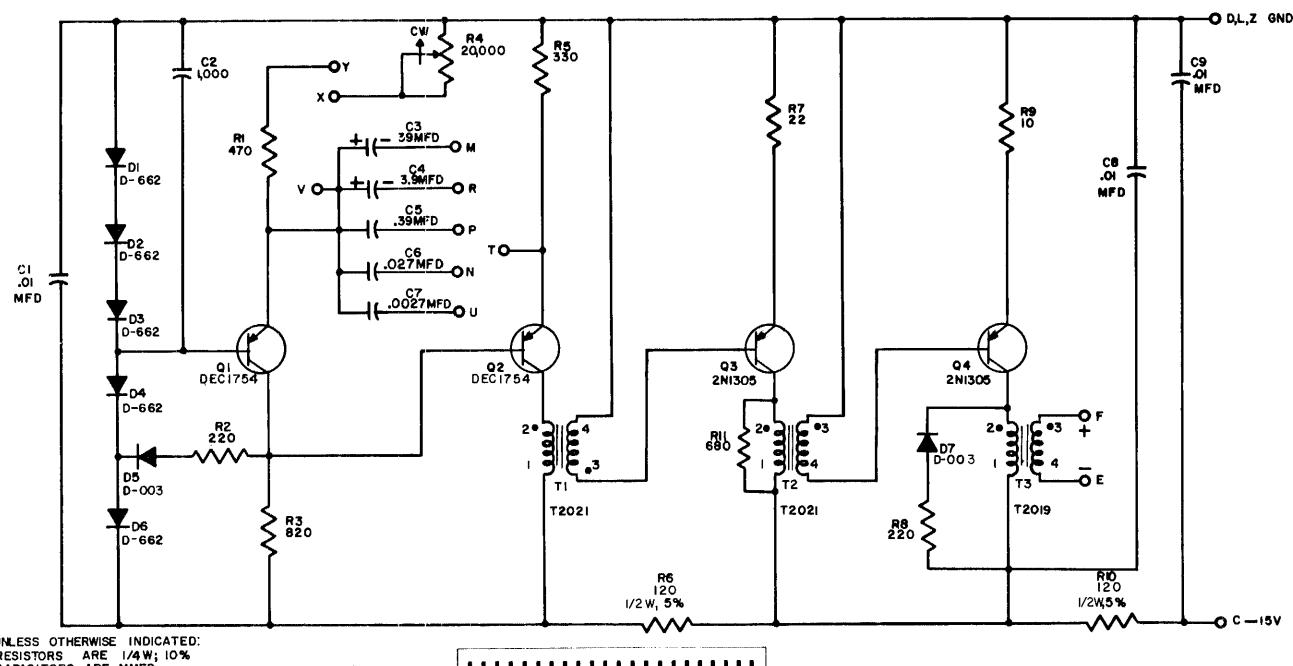
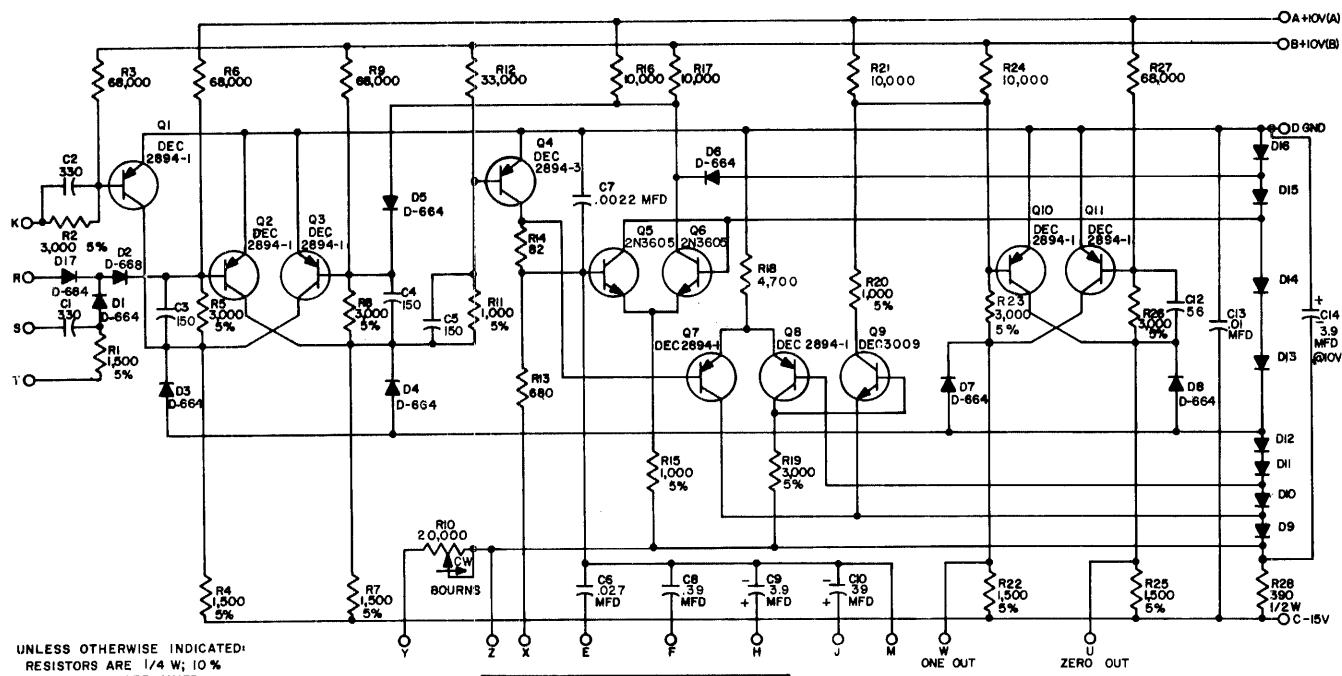
4-Bit Counter RS-4215

Quadruple Flip-Flop RS-4216



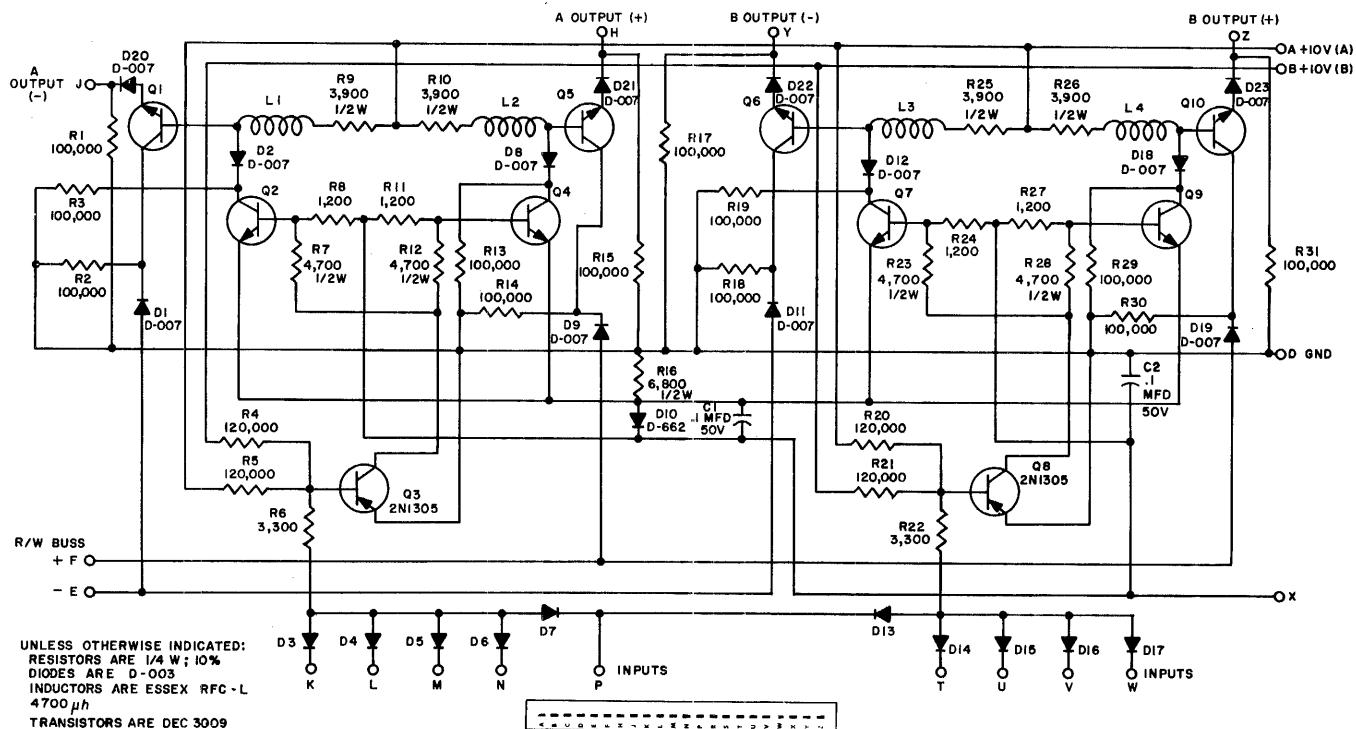
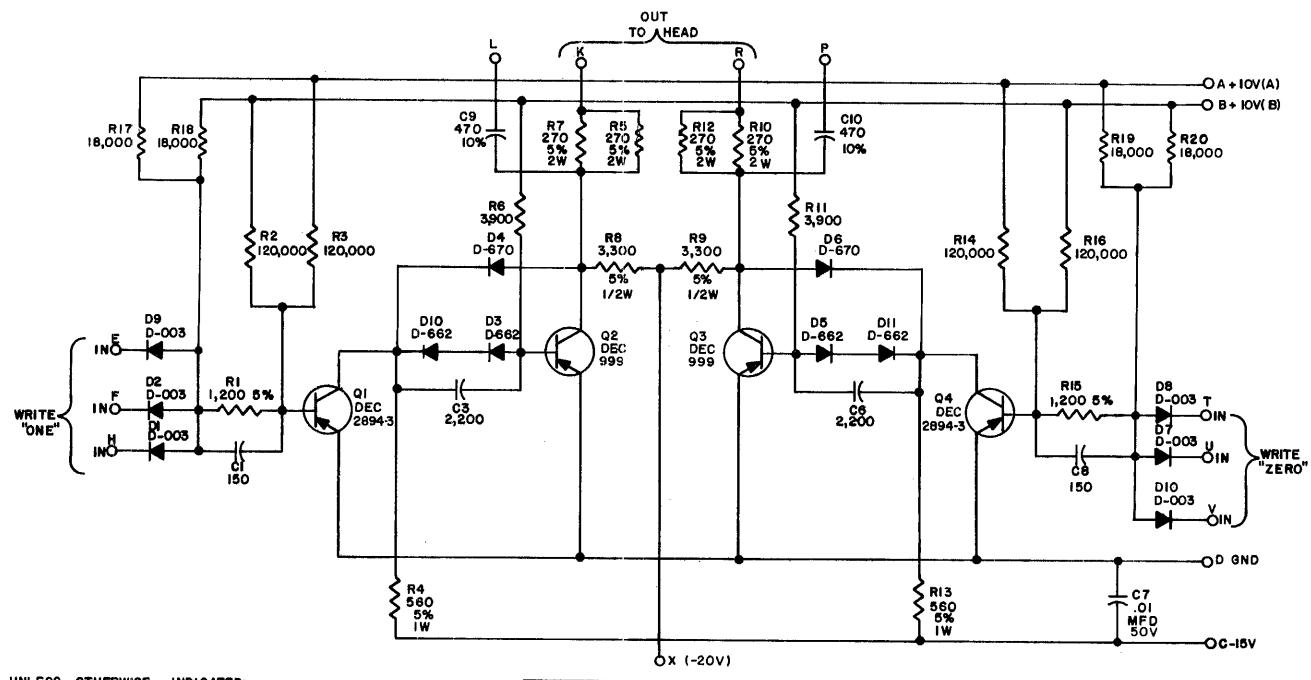
4-Bit Counter RS-4217

Delay RS-4301



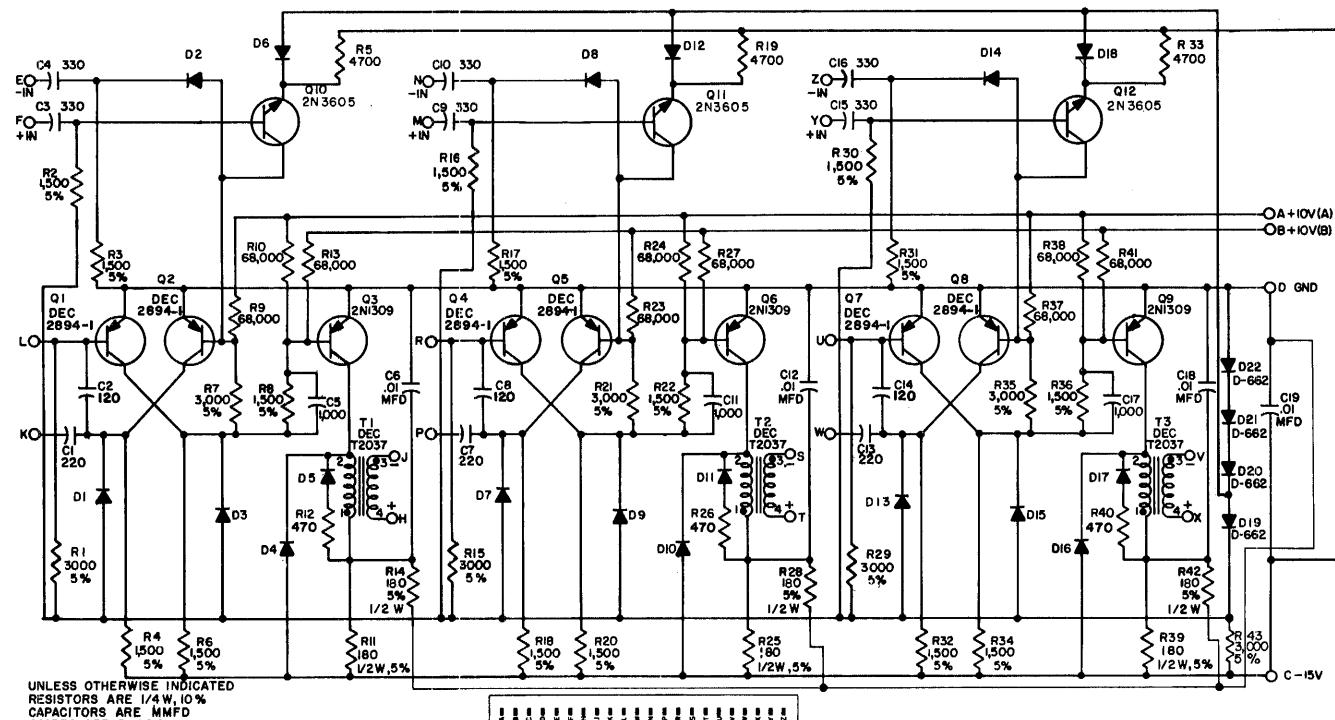
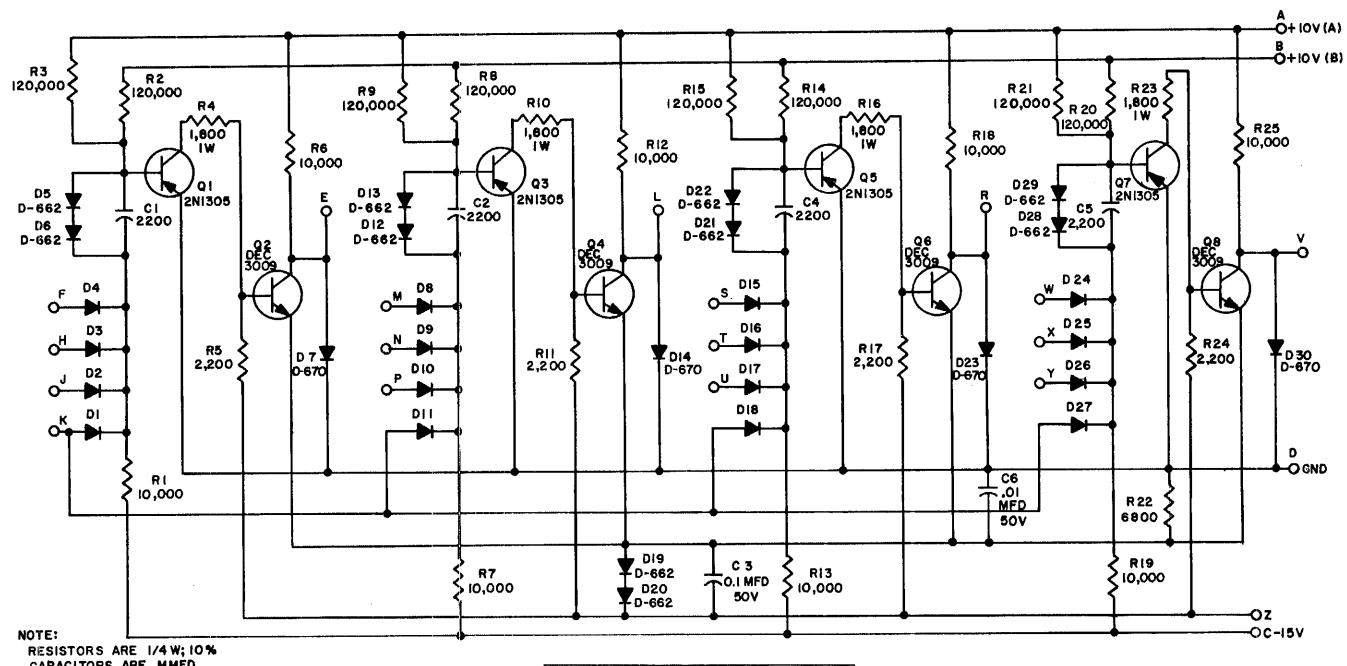
Integrating One-Shot RS-4303

Clock RS-4401



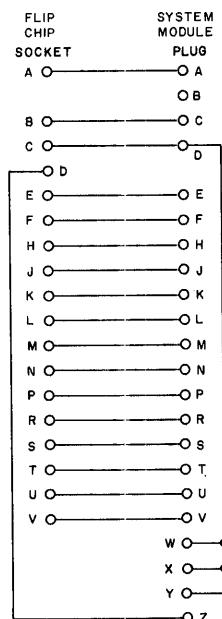
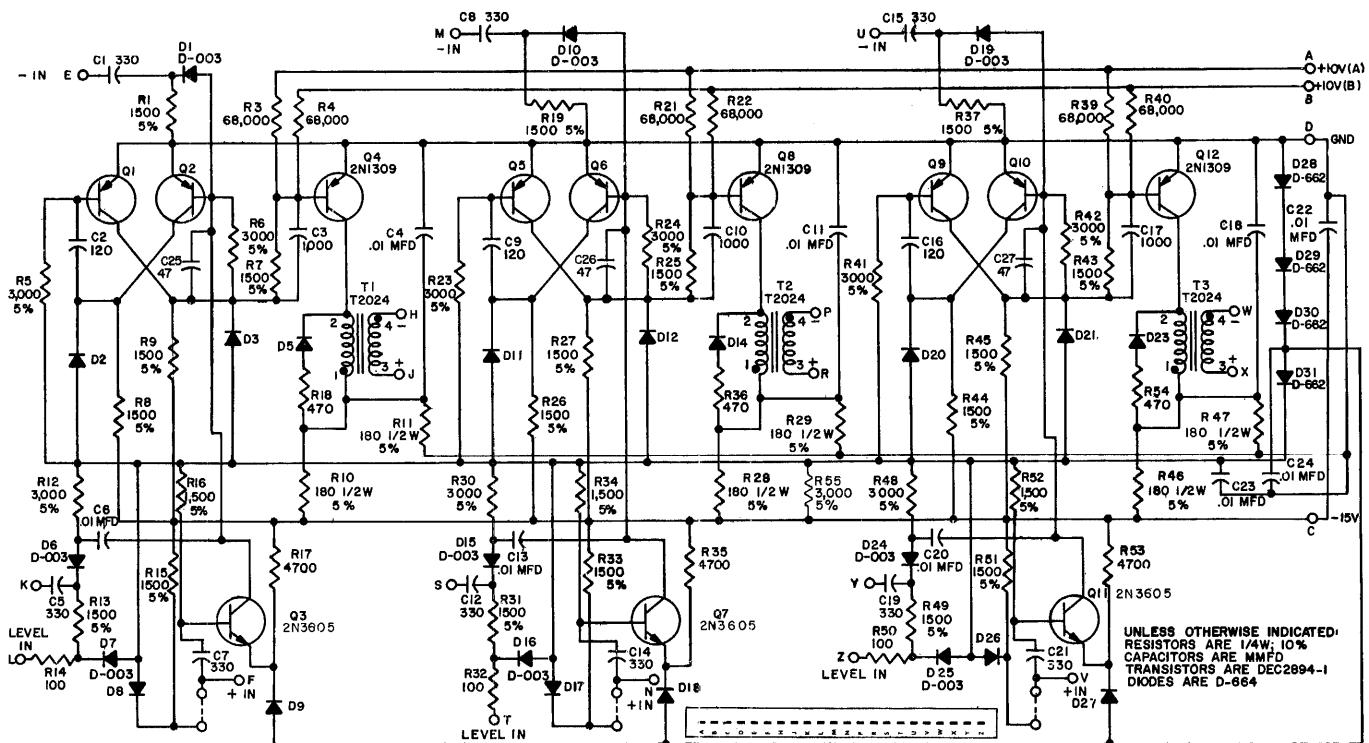
Drum NRZ Writer RS-4529

Drum X Select RS-4530



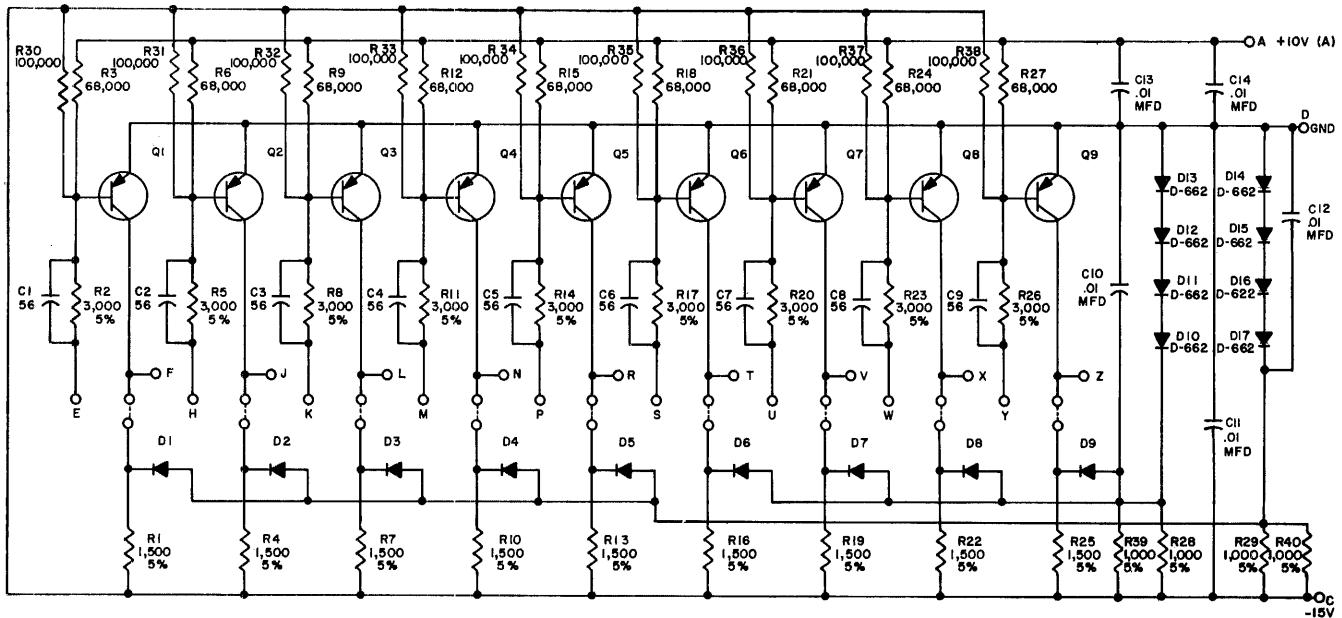
Drum Y Select RS-4531

Pulse Amplifier RS-4604

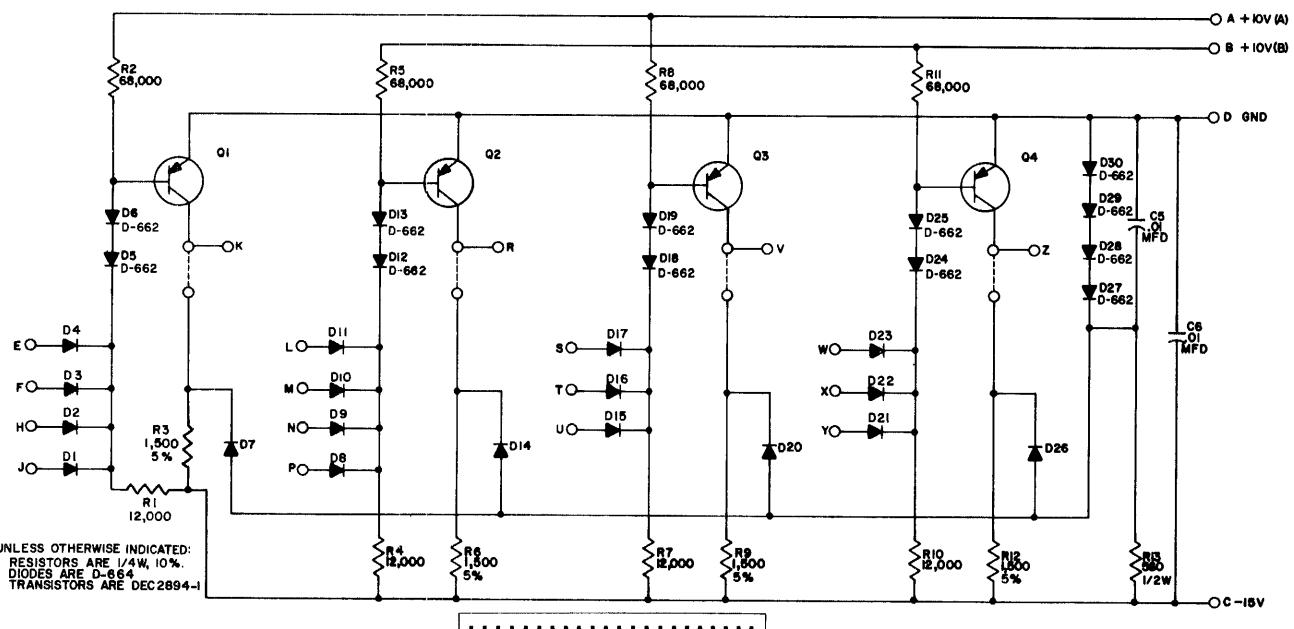


Pulse Amplifier RS-4606

FLIP CHIP Adapter RS-4912



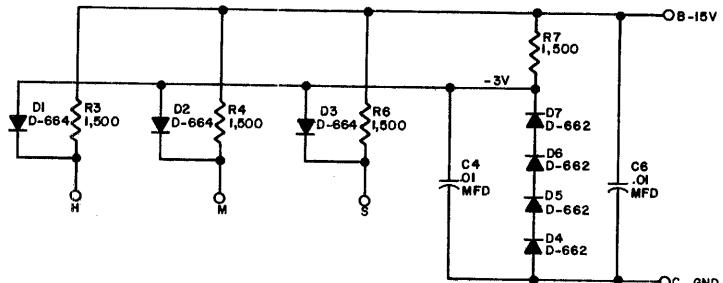
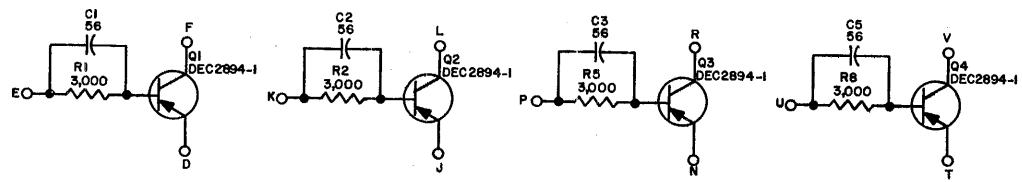
UNLESS OTHERWISE INDICATED
 RESISTORS ARE 1/4W, 10%
 CAPACITORS ARE MFD
 TRANSISTORS ARE DEC 2894-I
 DIODES ARE D-664



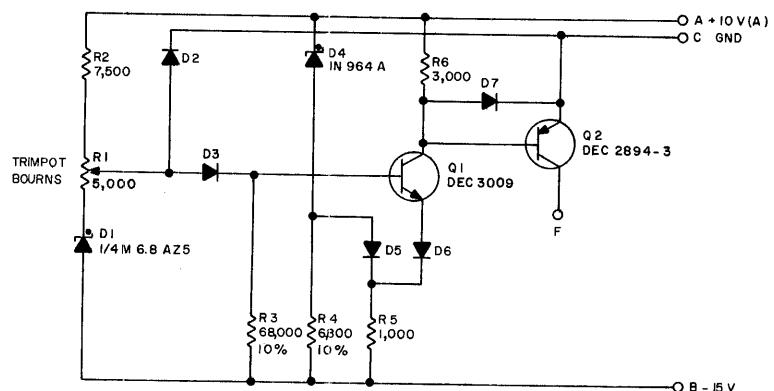
UNLESS OTHERWISE INDICATED:
 RESISTORS ARE 1/4W, 10%
 DIODES ARE D-662
 TRANSISTORS ARE DEC 2894-I

Inverter RS-6102

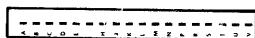
Diode RS-6115



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 5%
CAPACITORS ARE MFD



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 5%
DIODES ARE D-664



Inverter RS-B104

NOTE: 1N964A -13v, 10%
Low Voltage Detector RS-W505

APPENDIX 1

The diagnostic test given as a corrective maintenance tool in Chapter 6 is for use with a PDP-4 computer which has the following standard subroutines stored in core memory. The routines allow automatic printing of test results on the Type 65 Printer-Keyboard. These routines are presented here to allow generation of a binary tape to store them in the PDP-4 if they are not present, or to allow comparison to determine the extent of modifications required in the diagnostic program to allow it to function with existing subroutines.

/TELETYPE SUBROUTINES, OCTAL AND DECIMAL FRACTIONAL PRINTS

/URNS INTERRUPT OFF

/OCTAL PRINT, WITH ZERO SUPPRESSION

/FORMAT LAC WD

/ TWORDZ
/ n /n=NUMBER OF DIGITS TO PRINT FROM
/LEFT END OF WORD

OCTAL

TWORDZ=JMS .

0
DAC DCPNUM
LAC (SZA)
DAC TWORDZ+17-JMS
LAC I TWORDZ-JMS
CMA
DAC DCPCNT
ISZ DCPCNT
ISZ TWORDZ-JMS
LAC DCPNUM
RTL
RAL
DAC DCPNUM
RAL
AND (7)
SZA
JMP TWORDZ+25- IMS

ISZ DCPCNT
JMP TWORDZ+11-JMS
TDIGIT
JMP I TWORDZ-JMS
DAC DCPD^TG
LAC (JMP TWORDZ+31-JMS)
DAC TWORDZ+17-JMS
LAC DCPDIG
TDIGIT
ISZ DCPCNT
JMP TWORDZ+11-JMS
JMP I TWORDZ-JMS

/OCTAL PRINT, NO ZERO SUPPRESSION

/FORMAT SAME AS TWORDZ

TWORD=JMS .

0
DAC DCPNUM
LAC TWORD-JMS
DAC TWORDZ-JMS
LAC (JMP TWORDZ+31-JMS)
JMP TWORDZ+3-JMS

/TABLE FOR OCTAL TO DECIMAL CONVERSION

DECIMAL

DCPTAB,	100000	10000	1000	100	10	1
---------	--------	-------	------	-----	----	---

OCTAL

/TELETYPE OUTPUT PACKAGE 0-1 9-26-62

EXT=JMP I-JMS TTAB=10

/TYPE 1 CHARACTER FROM AC BITS 12-17

TY1=JMS .

0
RAR
JMS TY1A
EXT TY1

/TYPE 1 CHARACTER (5 BIT), LINK INDICATES CASE

TY1A, 0
DAC TEMY
AND (37
SNA
JMP TY2
LAC OCL
SPL
LAC OCU
SAD OCS
JMP . 3
JMS OTY
DAC OCS
LAC TEMY
JMS OTY
ISZ TBC
TY2, LAC TEMY
JMP I TY1A

/TYPE 3 CHARACTERS FROM AC 0-5, 6-11, 12-17 RESPECTIVELY

TY3=JMS .

0
JMS R16
JMS TY1A
JMS R16
JMS TY1A
JMS R16
JMS TY1A
EXT TY3

/TYPE A CARRIAGE RETURN, AND LINE FEED

TCR = JMS .

0
LAW 2
JMS OTY
LAW 10
JMS OTY
DZM TBC
EXT TCR

/TELETYPE OUTPUT PACKAGE - PAGE 2

/TYPE A SPACE

TSP=JMS .

0

LAW 4

JMS OTY

ISZ TBC

EXT TSP

/TYPE A TABULATION

TYT=JMS .

TAB=TYT

0

LAC TBC

ADD (-TTAB-1

SMA

JMP .-2

ADD (1

SMA

LAC (-TTAB-1

ADD (-1

DAC TEM

TSP

ISZ TEM

JMP .-2

EXT TYT

/TYPEWRITER INITIALIZE

TIN=JMS .

0

LAC OCL

DAC OCS

JMS OTY

TCR

EXT TIN

/TYPE THE DIGIT IN THE AC

TDIGIT-JMS .

0
AND (17
ADD (LAC NCT
DAC .1
XX
TY1
EXT TDIGIT
/TELETYPE OUTPUT PACKAGE - PAGE 3
/TYPE A STRING OF CHARACTERS
TSR=JMS .
0
DAC TEMY1
LAC (JMP TSR1
DAC TY1A 4
LAC I TEMY1
TY3
ISZ TEMY1
JMP .-3
TSR1, LAC (JMP TY2
DAC TY1A 4
LAC TEMY1
EXT TSR
/OUTPUT ONE FIVE-BIT CHARACTER
OTY, 0
IOF
DAC TWORD-JMS /SAVE
LAW /COUNTER
DAC R16
LAC TWORD-JMS
TSF
SKP
JMP .+3
ISZ R16
JMP .-4
TLS
JMP I OTY

/ROTATE LEFT 6

R16, 0
RTL
RTL
RTL
JMP I R16

/TABLE OF DIGITS

NCT,	33	73	63	41
	25	3	53	71
	31	7		

/CASE STORAGE

OCU, 33
OCL, 37
OCS, 0

/DECIMAL FRACTIONAL PRINT SUBROUTINE

/USES TELETYPE OUTPUT PACKAGE

/SUPPRESSES UNNECESSARY ZEROS

/FORMAT LAC NUMBER
/ DECFR
/ X /NUMBER OF DECIMAL PLACES (0-6)
DECFR=JMS .

0
SMA V CCL
CMA V CLL /MAKE WORD NEGATIVE
DAC DCPNUM
LAW CHAR R /SPACE
SZL
LAW CHAR R- /MINUS
TY1
LAC (ADD DCPTAB)
DAC DECFR1+2
LAM -5
DAC DCPCNT
LAC I DECFR-JMS
ISZ DECFR-JMS
ADD .-4 /-5

DAC DCPCN1
SMA
JMP DECFR6 /WRITE INITIAL ZERO
LAC (SZA)
DAC DECFR2
DZM DCPDTG /VALUE COUNTER
LAC DCPNUM
JMP .+3
DECFR1, DAC DCPNUM
ISZ DCPDIG
ADD DCPTAB /MODIFIED
SPA
JMP DECFR1
ISZ DECFR1+2
LAC DCPDIG
DECFR2, SZA /MODIFIED TO JMP DECFR3
JMP DECFR3
ISZ DCPCN1
JMP DECFR5
CLC
DAC DCPCN1
CLA
DECFR3, TDIGIT
ISZ DCPCNT
SKP
JMP 1 DECFR-JMS
DECFR4, LAC DECFR2+1
ISZ DCPCN1
JMP DECFR1-4
LAW CHAR R. /PERIOD
TY1
JMP DECFR4
DECFR5, ISZ DCPCNT
JMP DECFR1--2
TDIGIT /SHOULD NEVER REACH HERE

JMP I DECFR-JMS

DECFR6, CLA

TDIGIT

JMP DECFR4+3

START

APPENDIX 2

TELEPRINTER SUBROUTINES FOR PDP-1

type 24 drum test - pdp 1• 11 dec 64

```
define          swap
  rcr 777
  rcr 777
  term

define          count A,B
  isp A
  jmp B
  term

define          setup A,B
  law i B
  dac A
  term

/octal typeout - suppresses leading zeros
/calling sequence: lac number, jda opt

100/
opt,          0
  dap opx
  setup op2, 6
  stf 1
op1,          szf i 1
  tyo
  lio opt
  cla
  rcl 3s
  dio opt
  sza
  clf 1
  sza 1
  law 20
  swap
  count op2, op1
  tyo
  opx,          jmp .

ott,          0
  dap ott
  setup op2,6
ot2,          lio ott
  cla
  rcl 3s
  dio ott
  sza 1
```

```

law 20
swap
tyo
count op2,ot2
ot1,           jmp .

/drum test 3
beg,          szs 40
jmp rng-3
law pto
dac pha
clf 7
law i 10
dac ctr
szs 10
jsp tst
jsp spd
jmp wri
boo,          isp ctr
jmp .-3
law i 2
dac ctr
stf 4
rng,          dzm rdt
dzm wdt
rbl,          lac wca
dac tm3
rcn,          jsp rad
dac rnu
dac i tm3
idx tm3
sas wrn
jmp rcn
lio wca
dwr
lio wdt
dbl
jsp wtl
e1,          dcn
jsp wtl
e2,          idx wdt
lio rca
drd
lio rdt
dbl
jsp wtl
e3,          dcn
jsp wtl
e4,          jsp rcm
idx rdt
sas drs
jmp rbl
szs 40
jmp rng
isp ctr
jmp rng
jmp beg

```

```

rad,          dap b           /random number generator routine
  lac hi
  lio lo
  rcr 7s
  xor lo
  dac lo
  dio hi
b,          jmp

wtl,          dap wtx
  dtd
  jmp .-1
  dse
  jmp par
wtx,
rcm,          dap rcx           /data error test routine
  lac wca
  dac tm3
  lac rca
  dac tm6
  law i 6
  dac opp
rdd,          lac i tm6
  sas i tm3
  jsp ert
  idx tm6
  idx tm3
  sas wrl
  jmp rdd
  szf 4
  jmp big
rcx,
big,          /random number routine?
  jmp
  lac i tm6
  sas i tm3
  jsp ert
  idx tm6
  idx tm3
  sas wrn
  jmp big
  jmp rcx

tst,          dap tsx           /routine to use TW switches for data
  hlt
  lat
  dac tm1
  hlt
  lat
  dac dtā
tsx,          jmp

spd,          dap spx
  lac wca
  dac tm2
  dzm dta
  lio dta
  dio i tm2
  idx tm2

```

```

mdo,           lio i pha
  szs 10
  lio tm1
  dio i tm2
  idx tm2
  sas wr1
  jmp .-3
spx,           jmp

wri,           szs 10           /write routine
  jmp goo
  dzm dta
goo,           lio wca
  dwr
  lio dta
  dbl           /load track address and go
  jsp wtl
e5,           szs 20
  jmp rea
  idx dta
  szs 10
  jsp tsw
  dac i wca
  sas drs
  jmp goo
  jmp rea
tsw,           dap tax
  lat
  dac dta
tax,           jmp

rea,           szs 20
  jmp doo
  dzm dta
  lac dta
  dac i wca
doo,           lio rca
  drd
  lio dta
  dbl           /start reading
  jsp wtl

e6,           jsp rcm
  idx dta
  szs 20
  jsp tsw
  szs 10
  jmp wri
  dac i wca
  sas drs
  jmp doo
  idx pha
  jmp boo

/error routine

```

```

par,           szs 30           /surpress printout
  jmp wtx-2
  dsp
  jmp prt
  lio (flexo par           /parity error
  repeat 3,ril 6s           tyo
  jmp pr1
prt,           lio (flexo mis /miss error
  repeat 3,ril 6s           tyo
pr1,           lac wtx
  and (7777
  jda opt
  lio (36
  tyo
  lac wtx
  and (7777
  szf 4
  jmp pr2
  lac dta
  jmp pr3
pr2,           sub (e3-1
  spa           /skip if e3 or e4
  jmp pr4
  lac rdt
pr3,           jda opt
  lio (77
  tyo
  jmp wtx
pr4,           lac wdt
  jmp pr3

ert,           dap erx
  szs 30
  jmp erx
  lio (7734
  tyo
  rir 6s
  tyo
  lac dta           /track address
  szf 4           /random routine?
  lac rdt
  jda opt
  lio (36
  tyo
  lac tm6           /word number
  and ran
  jda opt
  lio (36
  tyo

md2,           lac i tm3
  szs 10

  lac tm1           /get data word written
  jda ott
  lio (3635
  tyo
  rir 6s
  tyo
  lac i tm6
  jda ott           /drum word

```

```
szs i 60      /prtn out more than 6 errors?
jmp . 4
isp opp
jmp . 2
xx
erx,          jmp .

/constants
wca,          2000
wrl,          2400
wrn,          3000
rca,          4000
rel,          4400
drs,          1000
pto,          777777
pt1,          000000
pt2,          111111
pt3,          222222
pt4,          333333
pt5,          444444
pt6,          555555
pt7,          666666
pha,          pto
ran,          777
hi,           365273
lo,           141053

dwr=721161
drd=720161
dbl=720162
dse=720164
dtd=720163
dcn=721162
dsp=721164

constants
variables
start beg
```

APPENDIX 3

SERIAL DRUM TYPE 24 INTERFACE WITH PDP-7 COMPUTER

For adaptation of some peripheral equipment the PDP-7 computer has a special adapter panel shown in Figure A3-1. Figure A3-2 details the conversion circuits for connection of Type 24 Drum signals to the PDP-7. The interface tables that follow detail all computer and drum connections to the interface panel.

TABLE A3-1 SERIAL DRUM 24D JACK F1 TO ADAPTER PANEL PLUG J1

Color	Pin	Pin	Name	Color	Pin	Pin	Name
WHT	3G11-R1-C	1	DFB ⁰ → MB ⁰	WHT	3G11-R2-V	18	DFB ¹⁷ → MB ¹⁷
WHT	3G11-R1-E	2	1	WHT	3G4-F	19	MBB ⁰ → DF ⁰
WHT	3G11-R1-G	3	2	WHT	3G4-J	20	1
WHT	3G11-R1-J	4	3	WHT	3G4-L	21	2
WHT	3G11-R1-L	5	4	WHT	3G4-N	22	3
WHT	3G11-R1-N	6	5	WHT	3G4-R	23	4
WHT	3G11-R1-R	7	6	WHT	3G4-T	24	5
WHT	3G11-R1-T	8	7	WHT	3G4-V	25	MBB ⁶ → DF ⁶
WHT	3G11-R1-V	9	8	WHT	3G4-X	26	MBB ⁷ → DF ⁷
WHT	3G11-R2-C	10	9	WHT	3G4-Z	27	8
WHT	3G11-R2-E	11	10	WHT	3G5-F	28	9
WHT	3G11-R2-G	12	11	WHT	3G5-J	29	10
WHT	3G11-R2-J	13	12	WHT	3G5-L	30	11
WHT	3G11-R2-L	14	13	WHT	3G5-N	31	12
WHT	3G11-R2-N	15	14	WHT	3G5-R	32	13
WHT	3G11-R2-R	16	15	WHT	3G5-T	33	14
WHT	3G11-R2-T	17	16	WHT	3G5-V	34	15

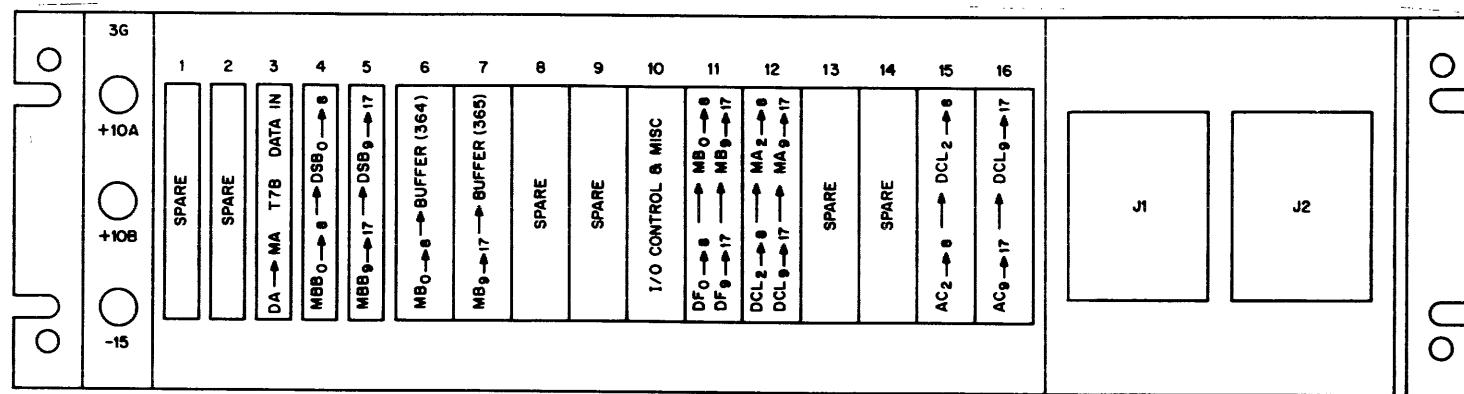


Figure A3-1 PDP-7 to Type 24 Drum Adapter Panel

A3-2

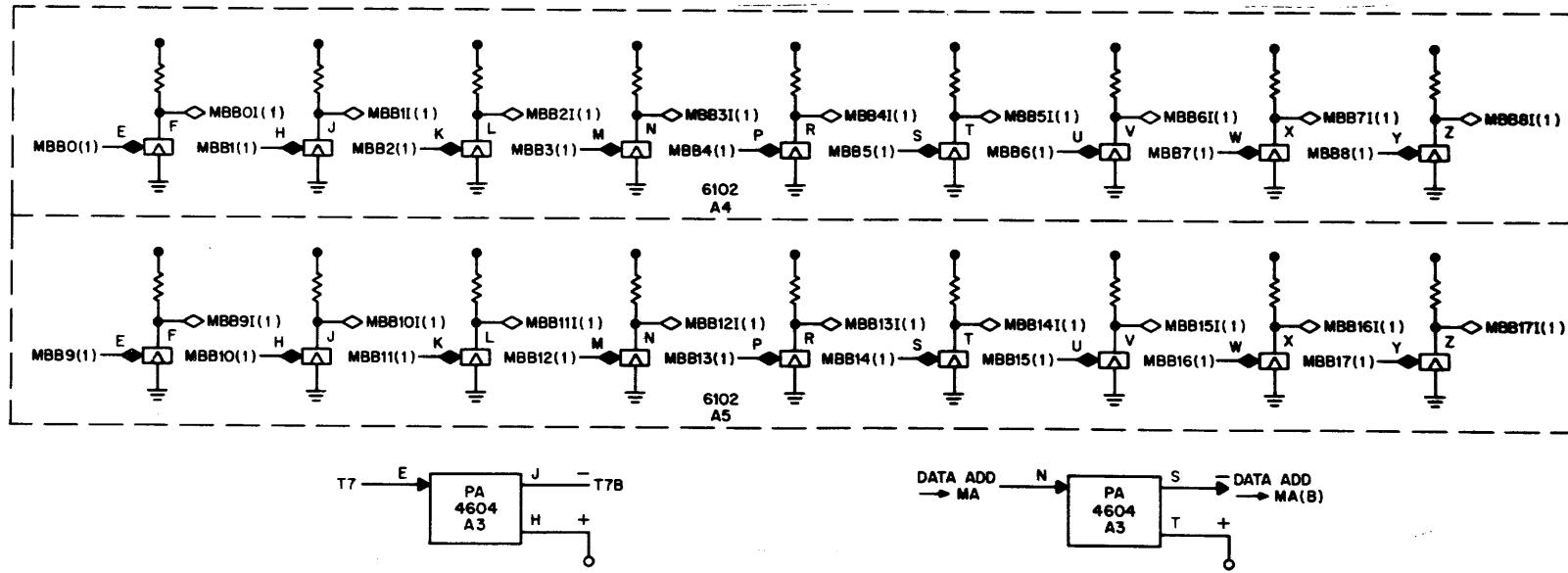


Figure A3-2 Type 24 Drum Interface to PDP-7

TABLE A3-1 SERIAL DRUM 24D JACK F1 TO ADAPTER PANEL PLUG J1 (continued)

Color	Pin	Pin	Name	Color	Pin	Pin	Name
WHT	3G5-X	35	16	WHT	3G12-R2-G	43	11
WHT	3G5-Z	36	MBB ¹⁷ → DF ¹⁷	WHT	3G12-R2-J	44	12
WHT	3G12-R1-N	37	DCLB ⁵ → MA ⁵	WHT	3G12-R2-L	45	13
WHT	3G12-R1-R	38	6	WHT	3G12-R2-N	46	14
WHT	3G12-R1-T	39	7	WHT	3G12-R2-R	47	15
WHT	3G12-R1-V	40	8	WHT	3G12-R2-T	48	16
WHT	3G12-R2-C	41	9	WHT	3G12-R2-V	49	DCLB ¹⁷ → MA ¹⁷
WHT	3G12-R2-E	42	10	BLK	GND LUG	40	GND

TABLE A3-2 SERIAL DRUM 24F JACK J2 COMPUTER SIDE

Color	Pin	Pin	Name	Color	Pin	Pin	Name
		1		WHT	3G16-R1-J	13	12
		2		WHT	3G16-R1-L	14	13
WHT	3G15-R1-G	3	ACB ² → DCL ²	WHT	3G16-R1-N	15	14
WHT	3G15-R1-J	4	3	WHT	3G16-R1-R	16	15
WHT	3G15-R1-L	5	4	WHT	3G16-R1-T	17	16
WHT	3G15-R1-N	6	5	WHT	3G16-R1-V	18	ACB ¹⁷ → DCL ¹⁷
WHT	3G15-R1-R	7	6	WHT	3G10-R2-G	19	DRUM FLAG
WHT	3G15-R1-T	8	7	WHT	3G10-R2-J	20	PE ⁰ · DE ⁰
WHT	3G15-R1-V	9	8	WHT	3G10-R2-L	21	DATA REQ
WHT	3G16-R1-C	10	9	WHT	3G10-R2-N	22	DATA IN
WHT	3G16-R1-E	11	10	WHT	3G12-R1-G	23	DCL ² → MA ²
WHT	3G16-R1-G	12	11	WHT	3G12-R1-J	24	DCL ³ → MA ³

TABLE A3-2 SERIAL DRUM 24F JACK J2 COMPUTER SIDE (continued)

Color	Pin	Pin	Name	Color	Pin	Pin	Name
WHT	3G12-R1-L	25	DCL ⁴ → MA ⁴			39	
		26				40	
		27				41	
		28		GRY			
		29		BLK	TWP	3G3-S	42 DATA REQ ANS
		30		GRY	TWP	3G10-R1-N	43 BEGIN
		31		BLK	TWP	3G3-J	44 T7B
		32		GRY	TWP	3G10-R1-C	45 IOT
		33		BLK	TWP	3G10-R1-E	46 IOT
		34		GRY	TWP	3G10-R1-G	47 IOT
WHT BLK	TWP	3G10-R2-C	35 TEMP SW (TA)	GRY	TWP	3G10-R1-J	48 IOT
		3G10-R2-E	36 TA GND	BLK	TWP	3G10-R1-L	49 IOT
		37		GRY			
RED	3G10-R2-R	38	+10 MC	BLK	GND	50	GND

TABLE A3-3 SERIAL DRUM 24D INTERFACE COMPUTER SIDE MB INVERSIONS

Color	Name	Pin	Pin	Remarks
WHT	MB ₀ ¹	3G6-R1-C	3G4-E	BUSS PINS
WHT	1	3G6-R1-E	3G4-H	B, D, F, H, K, M,
WHT	2	3G6-R1-G	3G4-K	P, S, U, & W to
WHT	3	3G6-R1-J	3G4-M	GROUND.
WHT	4	3G6-R1-L	3G4-P	

TABLE A3-3 SERIAL DRUM 24D INTERFACE
COMPUTER SIDE MB INVERSIONS (continued)

Color	Name	Pin	Pin	Remarks
WHT	5	3G6-R1-N	3G4-S	
WHT	6	3G6-R1-R	3G4-U	
WHT	7	3G6-R1-T	3G4-W	
WHT	8	3G6-R1-V	3G4-Y	
WHT	9	3G7-R1-C	3G5-E	
WHT	10	3G7-R1-E	3G5-H	
WHT	11	3G7-R1-G	3G5-K	
WHT	12	3G7-R1-J	3G5-M	
WHT	13	3G7-R1-L	3G5-P	
WHT	14	3G7-R1-N	3G5-S	
WHT	15	3G7-R1-R	3G5-U	
WHT	16	3G7-R1-T	3G5-W	
WHT	MB ¹ ₁₇	3G7-R1-V	3G5-Y	
	T7	3G10-R2-T	3G3-E	
	DATA ADD → MA	3G10-R2-V	3G3-N	

TABLE A3-4 I/O INFO FROM DRUM INTERFACE F10(R2) TO 1N10

Color	Name	Pin	Location	Remarks
		A		BLANK
		B		BLANK
W/BLK	GND	C		
W/BRN	IOT 6101	D	3G10-R2-C	M13K
W/RED	GND		3G10-R2-D	

TABLE A3-4 I/O INFO FROM DRUM INTERFACE F10(R2) TO 1N10 (continued)

Color	Name	Pin	Location	Remarks
W/ORN	IOT 6201	E	3G10-R2-E	M13M
W/YEL	GND	F	3G10-R2-F	
W/GRN	DRUM FLG.	H	3G10-R2-G	M13L
W/BLU	GND	J	3G10-R2-H	
W/VIO	PE ⁰ ·DE ⁰ FLG	K	3G10-R2-J	M13N
W/GRY	GND	L	3G10-R2-K	
WHT	DATA REQ	M	3G10-R2-L	L17U
W/BLK	GND	N	3G10-R2-M	
W/BRN	DATA IN	P	3G10-R2-N	L18F
W/RED	GND	R	3G10-R2-P	
W/ORN		S	3G10-R2-R	
W/YEL	GND		3G10-R2-S	
W/GRN	T7	T	3G10-R2-T	K15N
W/BLU	GND	U	3G10-R2-U	
W/VIO	DATA ADD	V	3G10-R2-V	L16H
W/GRY	GND			

TABLE A3-5 ACB 0-8 FROM CPU TO DRUM INTERFACE

Color	Name	Pin	Location	Remarks
		A		BLANK
		B		BLANK
W/BLK	GND	C		
W/BRN	◇ACB 0	D	3G15C	R2
W/RED	GND		3G15D	R2
W/ORN	ACB 1	E	3G15E	R2

TABLE A3-5 ACB 0-8 FROM CPU TO DRUM INTERFACE (continued)

Color	Name	Pin	Location	Remarks
W/YEL	GND	F	3G15F	R2
W/GRN	ACB 2	H	3G15G	R2
W/BLU	GND	J	3G15H	R2
W/VIO	ACB 3	K	3G15J	R2
W/GRY	GND	L	3G15K	R2
WHT	ACB 4	M	3G15L	R2
W/BLK	GND	N	3G15M	R2
W/BRN	ACB 5	P	3G15N	R2
W/RED	GND	R	3G15P	R2
W/ORN	ACB 6	S	3G15R	R2
W/YEL	GND		3G15S	R2
W/GRN	ACB 7	T	3G15T	R2
W/BLU	GND	U	3G15U	R2
W/VIO	ACB 8	V	3G15V	R2
W/GRY	GND			

TABLE A3-6 AC 9-17 FROM CPU TO DRUM INTERFACE

Color	Name	Pin	Location	Remarks
		A		BLANK
		B		BLANK
W/BLK	GND	C		
W/BRN	ACB 9	D	3G16C	R1
W/RED	GND		3G16D	R1
W/ORN	ACB 10	E	3G16E	R1
W/YEL	GND	F	3G16F	R1

TABLE A3-6 AC 9-17 FROM CPU TO DRUM INTERFACE (continued)

Color	Name	Pin	Location	Remarks
W/GRN	ACB 11	H	3G16G	R1
W/BLU	GND	J	3G16H	R1
W/VIO	ACB 12	K	3G16J	R1
W/GRY	GND	L	3G16K	R1
WHT	ACB 13	M	3G16L	R1
W/BLK	GND	N	3G16M	R1
W/BRN	ACB 14	P	3G16N	R1
W/RED	GND	R	3G16P	R1
W/ORN	ACB 15	S	3G16R	R1
W/YEL	GND		3G16S	R1
W/GRN	ACB 16	T	3G16T	R1
W/BLU	GND	U	3G16U	R1
W/VIO	ACB 17	V	3G16V	R1
W/GRY	GND			

TABLE A3-7 DFB 0-17 TO MB 0-17

Color	Name	Pin	Location	Remarks
		A		BLANK
		B		BLANK
W/BLK	GND	C		
W/BRN	DFB 0	D	3G11-R1-C	
W/RED	GND		3G11-R1-D	
W/ORN	DFB 1	E	3G11-R1-E	
W/YEL	GND	F	3G11-R1-F	

TABLE A3-7 DFB 0-17 TO MB 0-17 (continued)

Color	Name	Pin	Location	Remarks
W/GRN	DFB 2	H	3G11-R1-G	
W/BLU	GND	J	3G11-R1-H	
W/VIO	DFB 3	K	3G11-R1-J	
W/GRY	GND	L	3G11-R1-K	
WHT	DFB 4	M	3G11-R1-L	
W/BLK	GND	N	3G11-R1-M	
W/BRN	DFB 5	P	3G11-R1-N	
W/RED	GND	R	3G11-R1-P	
W/ORN	DFB 6	S	3G11-R1-R	
W/YEL	GND		3G11-R1-S	
W/GRN	DFB 7	T	3G11-R1-T	
W/BLU	GND	U	3G11-R1-U	
W/VIO	DFB 8	V	3G11-R1-V	
W/GRY	GND			
		A		BLANK
		B		BLANK
W/BLK	GND	C		
W/BRN	DFB 9	D	3G11-R2-C	
W/RED	GND		3G11-R2-D	
W/ORN	DFB 10	E	3G11-R2-E	
W/YEL	GND	F	3G11-R2-F	
W/GRN	DFB 11	H	3G11-R2-G	
W/BLU	GND	J	3G11-R2-H	
W/VIO	DFB 12	K	3G11-R2-J	

TABLE A3-7 DFB 0-17 TO MB 0-17 (continued)

Color	Name	Pin	Location	Remarks
W/GRY	GND	L	3G11-R2-K	
WHT	DFB 13	M	3G11-R2-L	
W/BLK	GND	N	3G11-R2-M	
W/BRN	DFB 14	P	3G11-R2-N	
W/RED	GND	R	3G11-R2-P	
W/ORN	DFB 15	S	3G11-R2-R	
W/YEL	GND		3G11-R2-S	
W/GRN	DFB 16	T	3G11-R2-T	
W/BLU	GND	U	3G11-R2-U	
W/VIO	DFB 17	V	3G11-R2-V	
W/GRY	GND			

TABLE A3-8 MBB 0-17 FROM CPU TO DRUM INTERFACE

Color	Name	Pin	Location	Remarks
		A		BLANK
		B		BLANK
W/BLK	GND	C	3G6B	R1
W/BRN	MBB 0(1)	D	3G6C	R1
W/RED	GND		3G6D	R1
W/ORN	MBB 1	E	3G6E	R1
W/YEL	GND	F	3G6F	R1
W/GRN	MBB 2	H	3G6G	R1
W/BLU	GND	J	3G6H	R1
W/VIO	MBB 3	K	3G6J	R1

TABLE A3-8 MBB 0-17 FROM CPU TO DRUM INTERFACE (continued)

Color	Name	Pin	Location	Remarks
W/GRY	GND	L	3G6K	R1
WHT	MBB 4	M	3G6L	R1
W/BLK	GND	N	3G6M	R1
W/BRN	MBB 5	P	3G6N	R1
W/RED	GND	R	3G6P	R1
W/ORN	MBB 6	S	3G6R	R1
W/YEL	GND		3G6S	R1
W/GRN	MBB 7	T	3G6T	R1
W/BLU	GND	U	3G6U	R1
W/VIO	MBB 8	V	3G6V	R1
W/GRY	GND			
		A		BLANK
		B		BLANK
W/BLK	GND	C		
W/BRN	MBB 9	D	3G7C	R1
W/RED	GND		3G7D	R1
W/ORN	MBB 10	E	3G7E	R1
W/YEL	GND	F	3G7F	R1
W/GRN	MBB 11	H	3G7G	R1
W/BLU	GND	J	3G7H	R1
W/VIO	MBB 12	K	3G7J	R1
W/GRY	GND	L	3G7K	R1
WHT	MBB 13	M	3G7L	R1
W/BLK	GND	N	3G7M	R1

TABLE A3-8 MBB 0-17 FROM CPU TO DRUM INTERFACE (continued)

Color	Name	Pin	Location	Remarks
W/BRN	MBB 14	P	3G7N	R1
W/RED	GND	R	3G7P	R1
W/ORN	MBB 15	S	3G7R	R1
W/YEL	GND		3G7S	R1
W/GRN	MBB 16	T	3G7T	R1
W/BLU	GND	U	3G7U	R1
W/VIO	MBB 17	V	3G7V	R1
W/GRY	GND			

TABLE A3-9 DCL 2-17 TO MA 2-17

Color	Name	Pin	Location	Remarks
		A		BLANK
		B		BLANK
W/BLK	GND	C	3G12-R1-B	
W/BRN	DCL	D	3G12-R1-C	
W/RED	GND		3G12-R1-D	
W/ORN	DCL	E	3G12-R1-E	
W/YEL	GND	F	3G12-R1-F	
W/GRN	DCL 2	H	3G12-R1-G	
W/BLU	GND	J	3G12-R1-H	
W/VIO	DCL 3	K	3G12-R1-J	
W/GRY	GND	L	3G12-R1-K	
WHT	DCL 4	M	3G12-R1-L	
W/BLK	GND	N	3G12-R1-M	

TABLE A3-9 DCL 2-17 TO MA 2-17 (continued)

Color	Name	Pin	Location	Remarks
W/BRN	DCL 5	P	3G12-R1-N	
W/RED	GND	R	3G12-R1-P	
W/ORN	DCL 6	S	3G12-R1-R	
W/YEL	GND		3G12-R1-S	
W/GRN	DCL 7	T	3G12-R1-T	
W/BLU	GND	U	3G12-R1-U	
W/VIO	DCL 8	V	3G12-R1-V	
W/GRY	GND		3G12-R1-W	
		A		BLANK
		B		BLANK
W/BLK	GND	C	3G12-R2-B	
W/BRN	DCL 9	D	3G12-R2-C	
W/RED	GND		3G12-R2-D	
W/ORN	DCL 10	E	3G12-R2-E	
W/YEL	GND	F	3G12-R2-F	
W/GRN	DCL 11	H	3G12-R2-G	
W/BLU	GND	J	3G12-R2-H	
W/VIO	DCL 12	K	3G12-R2-J	
W/GRY	GND	L	3G12-R2-K	
WHT	DCL 13	M	3G12-R2-L	
W/BLK	GND	N	3G12-R2-M	
W/BRN	DCL 14	P	3G12-R2-N	
W/RED	GND	R	3G12-R2-P	
W/ORN	DCL 15	S	3G12-R2-R	

TABLE A3-9 DCL 2-17 TO MA 2-17 (continued)

Color	Name	Pin	Location	Remarks
W/YEL	GND		3G12-R2-S	
W/GRN	DCL 16	T	3G12-R2-T	
W/BLU	GND	U	3G12-R2-U	
W/VIO	DCL 17	V	3G12-R2-V	
W/GRY	GND		3G12-R2-W	

TABLE A3-10 I/O INFO TO DRUM INTERFACE TO D16 DS

Color	Name	Pin	Location	Remarks
		A		BLANK
		B		BLANK
W/BLK	GND	C		
W/BRN	IOT 6002	D	3G10-R1-C	
W/RED	GND		3G10-R1-D	
W/ORN	IOT 6004	E	3G10-R1-E	
W/YEL	GND	F	3G10-R1-F	
W/GRN	IOT 6102	H	3G10-R1-G	
W/BLU	GND	J	3G10-R1-H	
W/VIO	IOT 6104	K	3G10-R1-J	
W/GRY	GND	L	3G10-R1-K	
WHT	IOT 6204	M	3G10-R1-L	
W/BLK	GND	N	3G10-R1-M	
W/BRN	BEGIN	P	3G10-R1-N	
W/RED	GND	R	3G10-R1-P	
W/ORN	IOT 6101	S	3G10-R1-R	
W/YEL	GND		3G10-R1-S	

TABLE A3-10 I/O INFO TO DRUM INTERFACE TO D16 DS (continued)

Color	Name	Pin	Location	Remarks
W/GRN	IOT 6204	T	3G10-R1-T	
W/BLU	GND	U	3G10-R1-U	
W/VIO		V		
W/GRY	GND			

